LM3533 Complete Lighting Power Solution for Smartphone Handsets

1 Features

- Drives Two Parallel High-Voltage LED Strings for Display and Keypad Lighting
- High-Voltage Strings Capable of up to 40-V Output Voltage and up to 90% Efficiency
- Up to 30 mA per Current Sink (Both Backlight and Indicator)
- 14-Bit Equivalent Exponential Dimming With 8-Bit Programmable Backlight Code
- Selectable Analog ALS Input with 128 Programmable Gain-Setting Resistors or PWM ALS Input With Internal Low-Pass Filter
- PWM Input for Content Adjustable Brightness Control
- Five Low-Voltage Current Sinks for Indicator LEDs
- Integrated Charge Pump for Improved Efficiency and V_{IN} Operating Range
- Internal Pattern Generation Engine
- Fully Configurable LED Grouping and Control
- Four Programmable Overvoltage Protection Thresholds (16 V, 24 V, 32 V, and 40 V)
- Programmable 500-kHz and 1-MHz Switching Frequency
- 27-mm^2 Total Solution Size

2 Applications

- Power Source for Smart Phone Illumination
- Display, Keypad and Indicator Illumination
- RGB Indicator Driver

3 Description

The LM3533 is a complete power source for backlight, keypad, and indicator LEDs in smartphone handsets. The high-voltage inductive boost converter provides the power for two series LED strings for display backlight and keypad functions (HVLED1 and HVLED2). The integrated charge pump provides the bias for the five low-voltage indicator LED current sinks (LVLED1 to LVLED5). All low-voltage current sinks can have a programmable pattern modulated onto their output current for a wide variety of blinking patterns.

Additional features include a pulse width modulation (PWM) control input for content adjustable backlight control (CABC), and an ambient light sensor interface (ALS) with an internal 8-bit ADC to provide automatic current adjustment based upon ambient light conditions. Both the PWM and ALS inputs can be used to control any high- or low-voltage current sink.

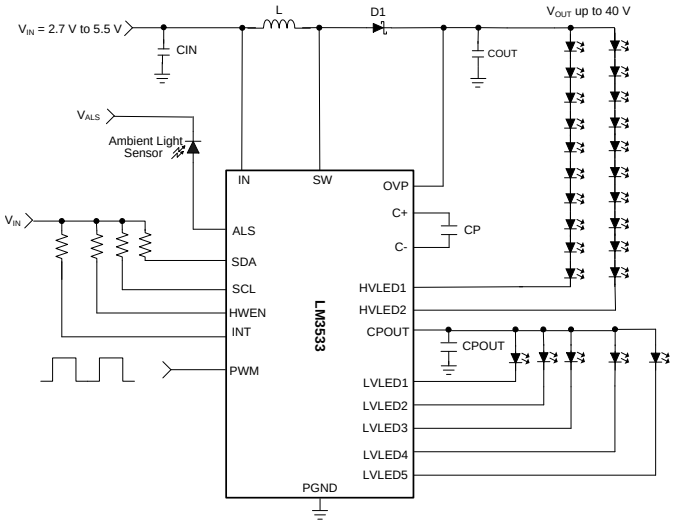
The LM3533 is fully programmable via an I^{2}C-compatible interface. The device is available in a 20-pin DSBGA and operates over a 2.7-V to 5.5-V input voltage range and a −40°C to +85°C temperature range.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (MAX)
LM3533	DSBGA (20)	2.04 mm × 1.78 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (May 2013) to Revision C **Page**

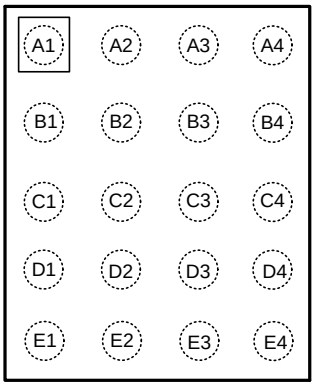
- Added *Device Information* and *Pin Configuration and Functions* sections, *ESD Rating* table, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections ... 1

Changes from Revision A (May 2013) to Revision B **Page**

- Changed layout of National Data Sheet to TI format ... 55

5 Pin Configuration and Functions

YFQ Package
20-Pin DSBGA
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
A1	C−	OUT	Integrated charge pump flying capacitor negative terminal. Connect a 1-µF ceramic capacitor from C+ to C−.
A2	C+	OUT	Integrated charge pump flying capacitor positive terminal. Connect a 1-µF ceramic capacitor from C+ to C−.
A3	CPOUT	OUT	Integrated charge pump output terminal. Bypass CPOUT to GND with a 1-µF ceramic capacitor.
A4	IN	IN	Input voltage connection. Bypass IN to GND with a minimum 2.2-µF ceramic capacitor.
B1	SCL	IN	Serial clock connection for I^2C-compatible interface.
B2	SDA	I/O	Serial data connection for I^2C-compatible interface.
B3	OVP	IN	Overvoltage sense Input. Connect OVP to the positive terminal of the inductive boost's output capacitor (COUT).
B4	GND	GND	Ground
C1	HVLED1	IN	Input pin to high-voltage current sink 1 (40 V maximum). The boost converter regulates the minimum of HVLED1 and HVLED2 to 0.4 V.
C2	INT	OUT	ALS interrupt output (INT). When INT mode is enabled this pin becomes an open-drain output that pulls low when the ALS changes zones. On power-up, INT mode is disabled and is high impedance and must be tied high or low.
C3	PWM	IN	PWM brightness control input for CABC operation. PWM is a high-impedance input and cannot be left floating.
C4	SW	IN	Drain connection for the internal NFET. Connect SW to the junction of the inductor and the Schottky diode anode.
D1	HVLED2	IN	Input pin high-voltage current sink 2 (40 V maximum). The boost converter regulates the minimum of HVLED1 and HVLED2 to 0.4 V.
D2	ALS	IN	Ambient light sensor input.
D3	HWEN	IN	Hardware enable input. Drive this pin high to enable the device. Drive this pin low to force the device into a low power shutdown. HWEN is a high-impedance input and cannot be left floating.
D4	LVLED5	IN	Low-voltage current sink 5
E1	LVLED1	IN	Low-voltage current sink 1
E2	LVLED2	IN	Low-voltage current sink 2
E3	LVLED3	IN	Low-voltage current sink 3
E4	LVLED4	IN	Low-voltage current sink 4

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)(3)

	MIN	MAX	UNIT
V_{IN} to GND	−0.3	6	V
V_{SW}, V_{OVP}, V_{HVLED1}, V_{HVLED2} to GND	−0.3	45	V
V_{SCL}, V_{SDA}, V_{ALS}, V_{PWM} to GND	−0.3	6	V
V_{INT}, V_{HWEN}, V_{CPOUT} to GND	−0.3	6	V
V_{LVLED1}- V_{LVLED5}, to GND	−0.3	6	V
Continuous power dissipation	Internally limited		
Junction temperature, T_{J-MAX}		150	°C
Maximum lead temperature (soldering)	See(4)		
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pin.
(3) If Military/Aerospace specified devices are required, contact the TI Sales Office/Distributors for availability and specifications.
(4) For detailed soldering specifications and information, refer to Texas Instruments Application Note 1112: *DSBGA Wafer Level Chip Scale Package* (SNVA009) available at www.ti.com.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	NOM	MAX	UNIT
V_{IN} to GND	2.7		5.5	V
V_{SW}, V_{OVP}, V_{HVLED1}, V_{VHLED2} to GND	0		40	V
V_{LVLED1}- V_{LVLED5} to GND	0		6	V
Junction temperature (T_J)(2)(3)	−40		125	°C

(1) All voltages are with respect to the potential at the GND pin.
(2) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 140°C (typical) and disengages at T_J= 125°C (typical).
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by the equation: $T_{A-MAX} = T_{J-MAX-OP} – (R_{\theta JA} \times P_{D-MAX})$.

6.4 Thermal Information

THERMAL METRIC(1)		LM3533 YFQ (DSBGA) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	55.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) Junction-to-ambient thermal resistance ($R_{J\theta A}$) is taken from a thermal modeling result, performed under the conditions and guidelines set forth in the JEDEC standard JESD51-7. The test board is a 4-layer FR-4 board measuring 102 mm × 76 mm × 1.6 mm with a 2 × 1 array of thermal vias. The ground plane on the board is 50 mm × 50 mm. Thickness of copper layers are 36 µm/18 µm/18 µm/36 µm (1.5 oz/1 oz/1 oz/1.5 oz). Ambient temperature in simulation is 22°C in still air. Power dissipation is 1 W. The value of $R_{\theta JA}$ of this product in the DSBGA package could fall in a range as wide as 60°C/W to 110°C/W (if not wider), depending on PCB material, layout, and environmental conditions. In applications where high maximum power dissipation exists special care must be paid to thermal dissipation issues.

6.5 Electrical Characteristics

Unless otherwise specified V_{IN} = 3.6 V; typical limits are for T_A = 25°C and minimum and maximum limits apply over the full operating ambient temperature range (−40°C ≤ T_A ≤ +85°C).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{SHDN}	Shutdown current	2.7 V ≤ V_{IN} ≤ 5.5 V, HWEN = GND			1	5	µA
I_{LED_MIN}	Minimum LED current	Full-scale current = 20.2 mA Exponential mapping			9.5		µA
T_{SD}	Thermal shutdown				140		°C
	Hysteresis				15		
BOOST CONVERTER							
$I_{HVLED(1/2)}$	Output current regulation (HVLED1 or HVLED2)	2.7 V ≤ V_{IN} ≤ 5.5 V full-scale current = 20.2mA, brightness code = 0xFF		17	20.2	23	mA
I_{MATCH_HV}	HVLED1 to HVLED2 matching (1)	2.7 V ≤ V_{IN} ≤ 5.5 V	Both current sinks are assigned to Control Bank A	–2%	1%	2%	
V_{REG_CS}	Regulated current sink headroom voltage				400		mV
V_{HR_HV}	Minimum current sink headroom voltage for HVLED current sinks	I_{LED} = 95% of nominal full-scale current = 20.2 mA			190	250	mV
R_{DSON}	NMOS switch on resistance	I_{SW} = 500 mA			0.3		Ω
I_{CL_BOOST}	NMOS switch current limit	V_{IN} = 3.6 V		880	1000	1120	mA
V_{OVP}	Output overvoltage protection	ON threshold, 2.7 V ≤ V_{IN} ≤ 5.5 V OVP select bits = 11		39	40	41	V
		Hysteresis			1		
f_{SW}	Switching frequency	2.7 V ≤ V_{IN} ≤ 5.5 V	Boost frequency select bit = 0	450	500	550	kHz
			Boost frequency select bit = 1	900	1000	1100	
D_{MAX}	Maximum duty cycle				94%		
CHARGE PUMP							
$I_{LVLED(1/2/3/4/5)}$	Output current regulation (low-voltage current sinks)	2.7 V ≤ V_{IN} ≤ 5.5 V, full-scale current = 20.2 mA brightness code = 0xFF		17	20.2	23	mA
I_{MATCH_LV}	LVLED current sink matching (2)	2.7 V ≤ V_{IN} ≤ 5.5 V		–2%	1%	2%	
V_{HR_LV}	Minimum current sink headroom voltage for LVLED current sinks	I_{LED} = 95% of nominal, full-scale current = 20.2 mA			80	110	mV
V_{GTH}	Threshold for gain transition	V_{LVLED} falling			110		mV
I_{CL_PUMP}	Charge-pump current limit	3 V ≤ V_{IN} ≤ 5.5 V, output referred	1× gain	180	350		mA
			2× gain		240		
R_{OUT}	Charge-pump output resistance	1× gain			1.1		Ω
HWEN INPUT							
V_{HWEN}	Logic thresholds	Logic low		0		0.4	V
		Logic high		1.2		V_{IN}	
PWM INPUT							
V_{PWM_L}	Input logic low	2.7 V ≤ V_{IN} ≤ 5.5 V		0		400	mV
V_{PWM_H}	Input logic high	2.7 V ≤ V_{IN} ≤ 5.5 V		1.25		V_{IN}	V

(1) LED current sink matching between HVLED1 and HVLED2 is given by taking the difference between either (IHVLED1 or IHVLED2) and the average current between the two, and dividing by the average current between the two. This simplifies to (I_{HVLED1} (or IHVLED2) – $I_{HVLED(AVE)}$)/($I_{HVLED(AVE)}$) × 100. In this test, both HVLED1 and HVLED2 are assigned to Bank A.

(2) LED current sink matching in the low-voltage current sinks (LVLED1 through LVLED5) is given as the maximum matching value between any two current sinks, where the matching between any two low voltage current sinks (X and Y) is given as (I_{LVLEDX} (or I_{LVLEDY}) – $I_{AVE(X-Y)}$)/($I_{AVE(X-Y)}$) × 100. In this test all LVLED current sinks are assigned to Bank C.

Electrical Characteristics (continued)

Unless otherwise specified V_{IN} = 3.6 V; typical limits are for T_A = 25°C and minimum and maximum limits apply over the full operating ambient temperature range (−40°C ≤ T_A ≤ +85°C).

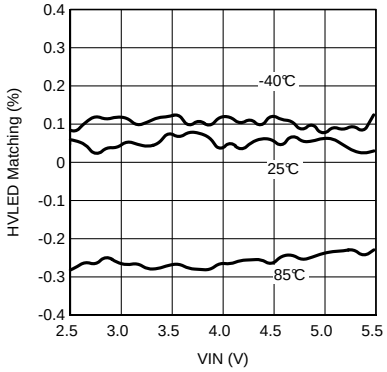
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INT OUTPUT						
V_{LOW}	Output Logic Low (INT Mode)	2.7 V ≤ V_{IN} ≤ 5.5 V			400	mV
I²C-COMPATIBLE VOLTAGE SPECIFICATIONS (SCL, SDA)						
V_{IL}	Input logic low	2.7 V ≤ V_{IN} ≤ 5.5 V	0		400	mV
V_{IH}	Input logic high	2.7 V ≤ V_{IN} ≤ 5.5 V	1.25		V_{IN}	V
V_{OL}	Output logic low (SDA)	I_{LOAD} = 3mA			400	mV
AMBIENT LIGHT SENSOR (ALS)						
R_{ALS}	ALS internal pulldown resistor in analog sensor input mode	R_ALS Select Register = 0x0F 2.7 V ≤ V_{IN} ≤ 5.5 V	12.36	13.33	13.94	kΩ
V_{ALS_REF}	Ambient Light Sensor Reference Voltage	2.7 V ≤ V_{IN} ≤ 5.5 V	1.9	2	2.1	V
V_{ALS_MIN}	Minimum Threshold for ALS Input Voltage Sensing	Analog sensor mode 2.7 V ≤ V_{IN} ≤ 5.5 V, Code 0 to 1 transition point	3	10	15	mV
t_{CONV}	Conversion Time			140		µs
LSB	ADC Resolution	2.7 V ≤ V_{IN} ≤ 5.5 V		7.8		mV

6.6 I²C Timing Requirements

		MIN	NOM	MAX	UNIT
t_1	SCL (Clock Period)	2.5			µs
t_2	Data In Setup Time to SCL High	100			ns
t_3	Data Out Stable After SCL Low	0			ns
t_4	SDA Low Setup Time to SCL Low (Start)	100			ns
t_5	SDA High Hold Time After SCL High (Stop)	100			ns

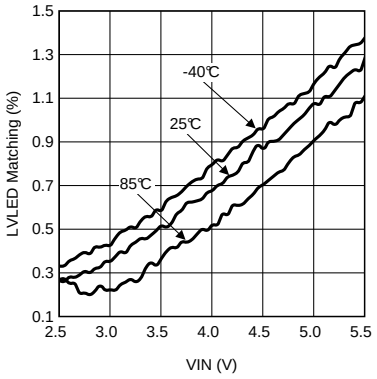
6.7 Typical Characteristics

V_{IN} = 3.6 V, LEDs are WLEDs part number SML-312WBCW(A), typical application circuit with L = TDK (VLF302512, 4.7 µH, 10 µH, 22 µH where specified), Schottky = On-Semi (NSR0240V2T1G), T_A = 25°C, unless otherwise specified. Efficiency is given as $V_{OUT} \times (I_{HVLED1} + I_{HVLED2})/(V_{IN} \times I_{IN})$; matching curves are given as $(\Delta I_{LED\_MAX}/I_{LED\_AVE})$.



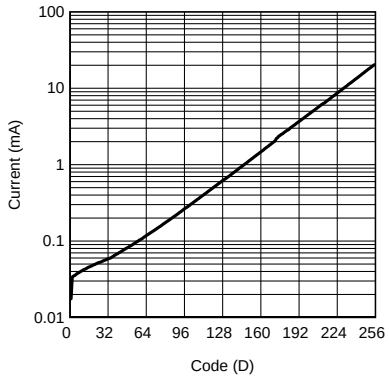
I_{LED} = 20 mA

Figure 1. HVLED Matching vs V_{IN}, Temp



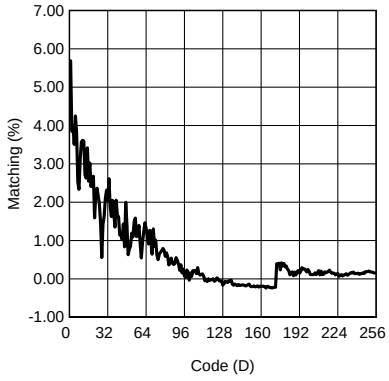
I_{LED} = 20 mA

Figure 2. LVLED Matching vs V_{IN}, Temp



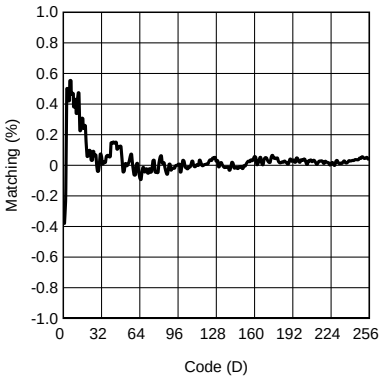
V_{IN} = 3.6 V

Figure 3. HVLED Current vs Code (Exponential Mode)



V_{IN} = 3.6 V

Figure 4. HVLED Matching vs Code (Exponential Mode)



V_{IN} = 3.6 V

Figure 5. HVLED Matching vs Code (Linear Mode)

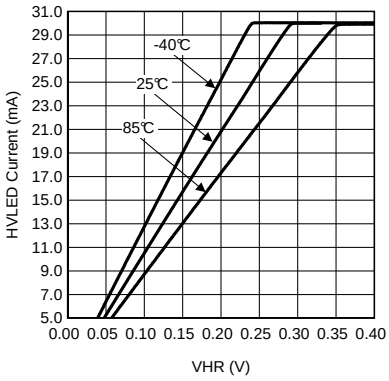


Figure 6. HVLED Current vs Current Sink Headroom Voltage

Typical Characteristics (continued)

V_{IN} = 3.6 V, LEDs are WLEDs part number SML-312WBCW(A), typical application circuit with L = TDK (VLF302512, 4.7 µH, 10 µH, 22 µH where specified), Schottky = On-Semi (NSR0240V2T1G), T_A = 25°C, unless otherwise specified. Efficiency is given as $V_{OUT} \times (I_{HVLED1} + I_{HVLED2})/(V_{IN} \times I_{IN})$; matching curves are given as $(\Delta I_{LED\_MAX}/I_{LED\_AVE})$.

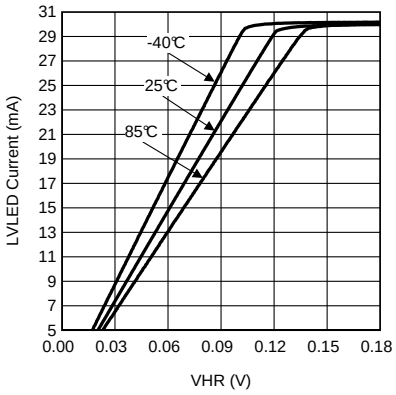
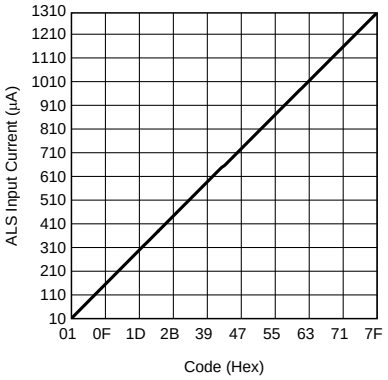


Figure 7. LVLED Current vs Current Sink Headroom Voltage



V_{ALS} = 2 V

Figure 8. ALS Input Current vs Code

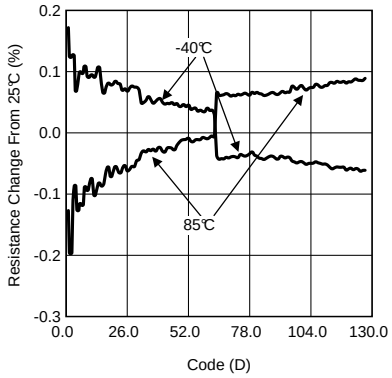
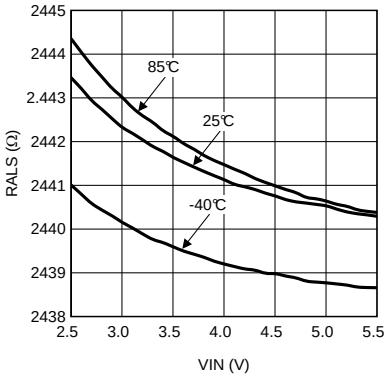


Figure 9. ALS Resistance vs Code (Temp)



(Code 0x50)

Figure 10. ALS Resistance vs V_{IN}

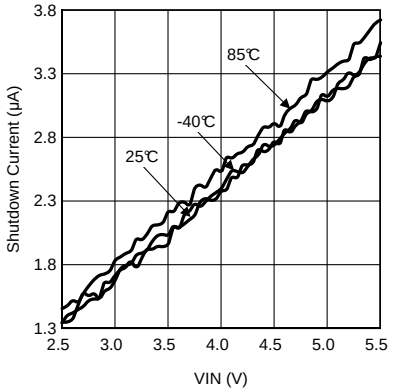


Figure 11. Shutdown Current vs V_{IN}

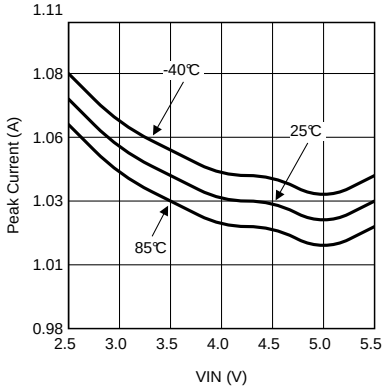
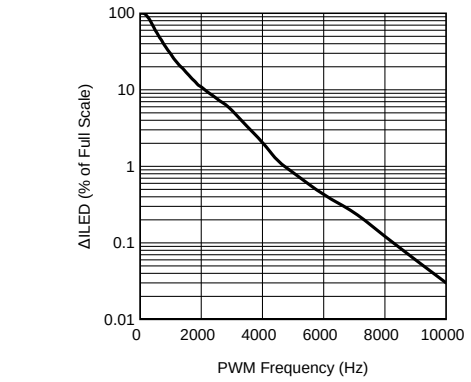


Figure 12. Closed Loop Current Limit vs V_{IN}

Typical Characteristics (continued)

V_{IN} = 3.6 V, LEDs are WLEDs part number SML-312WBCW(A), typical application circuit with L = TDK (VLF302512, 4.7 µH, 10 µH, 22 µH where specified), Schottky = On-Semi (NSR0240V2T1G), T_A = 25°C, unless otherwise specified. Efficiency is given as $V_{OUT} \times (I_{HVLED1} + I_{HVLED2})/(V_{IN} \times I_{IN})$; matching curves are given as $(\Delta I_{LED\_MAX}/I_{LED\_AVE})$.



50% Duty Cycle I_{LED} Full_scale = 20.2 mA

Figure 13. Led Current Ripple vs F_{PWM}

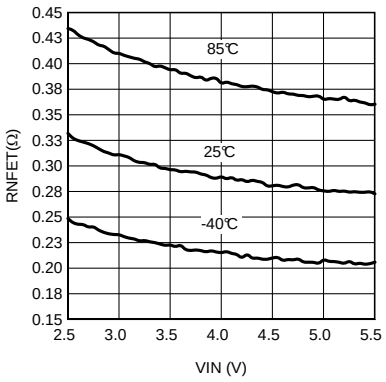
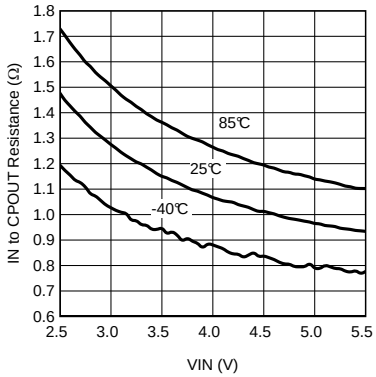
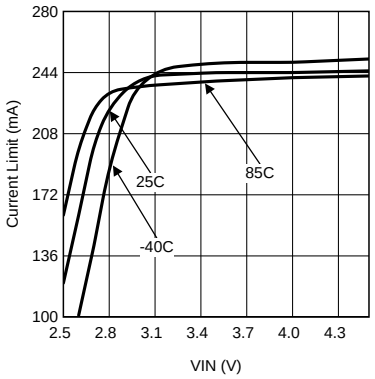


Figure 14. NMOS On Resistance vs VIN



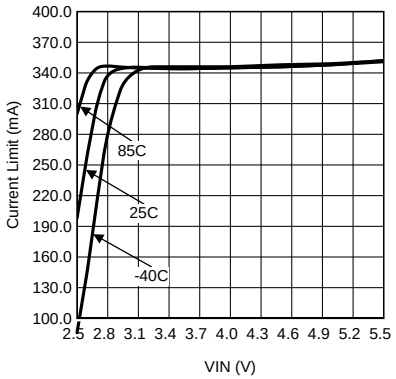
1x Gain

Figure 15. IN to CP_{OUT} Resistance vs V_{IN}



2× Gain

Figure 16. Charge Pump Short Circuit Current Limit vs V_{IN}



1× Gain

Figure 17. Charge Pump Short Circuit Current Limit vs V_{IN}

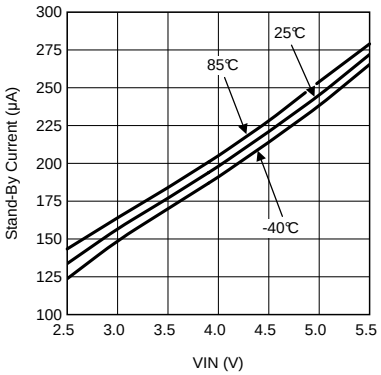
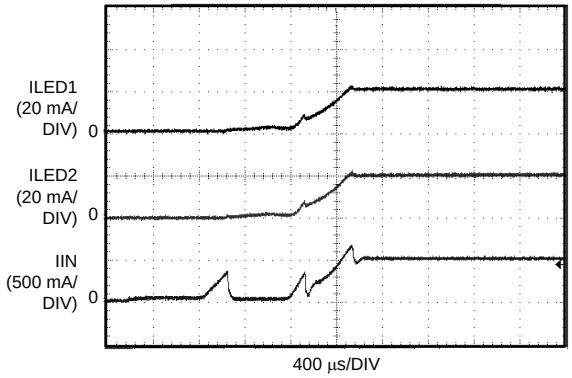


Figure 18. Idle State Supply Current (Pattern Generator Enabled On LVLED1, LVLED2, LVLED3)

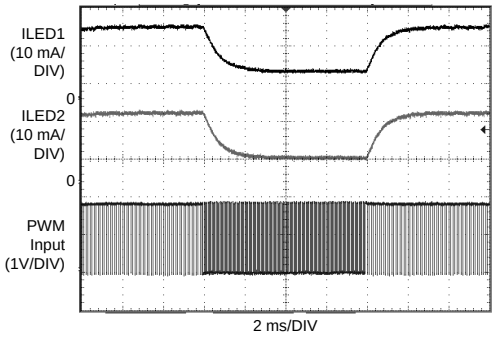
Typical Characteristics (continued)

V_{IN} = 3.6 V, LEDs are WLEDs part number SML-312WBCW(A), typical application circuit with L = TDK (VLF302512, 4.7 µH, 10 µH, 22 µH where specified), Schottky = On-Semi (NSR0240V2T1G), T_A = 25°C, unless otherwise specified. Efficiency is given as $V_{OUT} \times (I_{HVLED1} + I_{HVLED2})/(V_{IN} \times I_{IN})$; matching curves are given as $(\Delta I_{LED\_MAX}/I_{LED\_AVE})$.



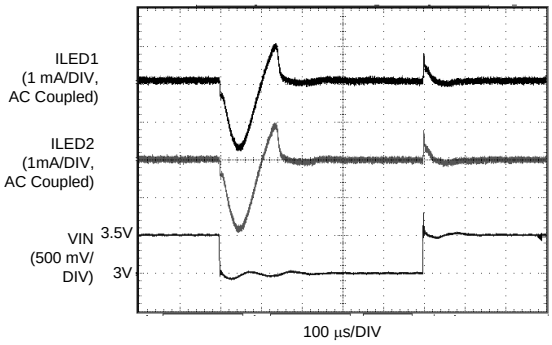
V_{IN} = 3.6 V 20 mA/String 2×8 LEDs

Figure 19. Start-Up Response



D = 30% To 90% f_{PWM} = 10 kHz
$I_{LED\_FULL\ SCALE}$ = 20.2 mA

Figure 20. Response To Step Change in PWM Input Duty Cycle



2×8 LEDs 20.2 mA/String

Figure 21. Line Step Response (see Typical Application Circuit)

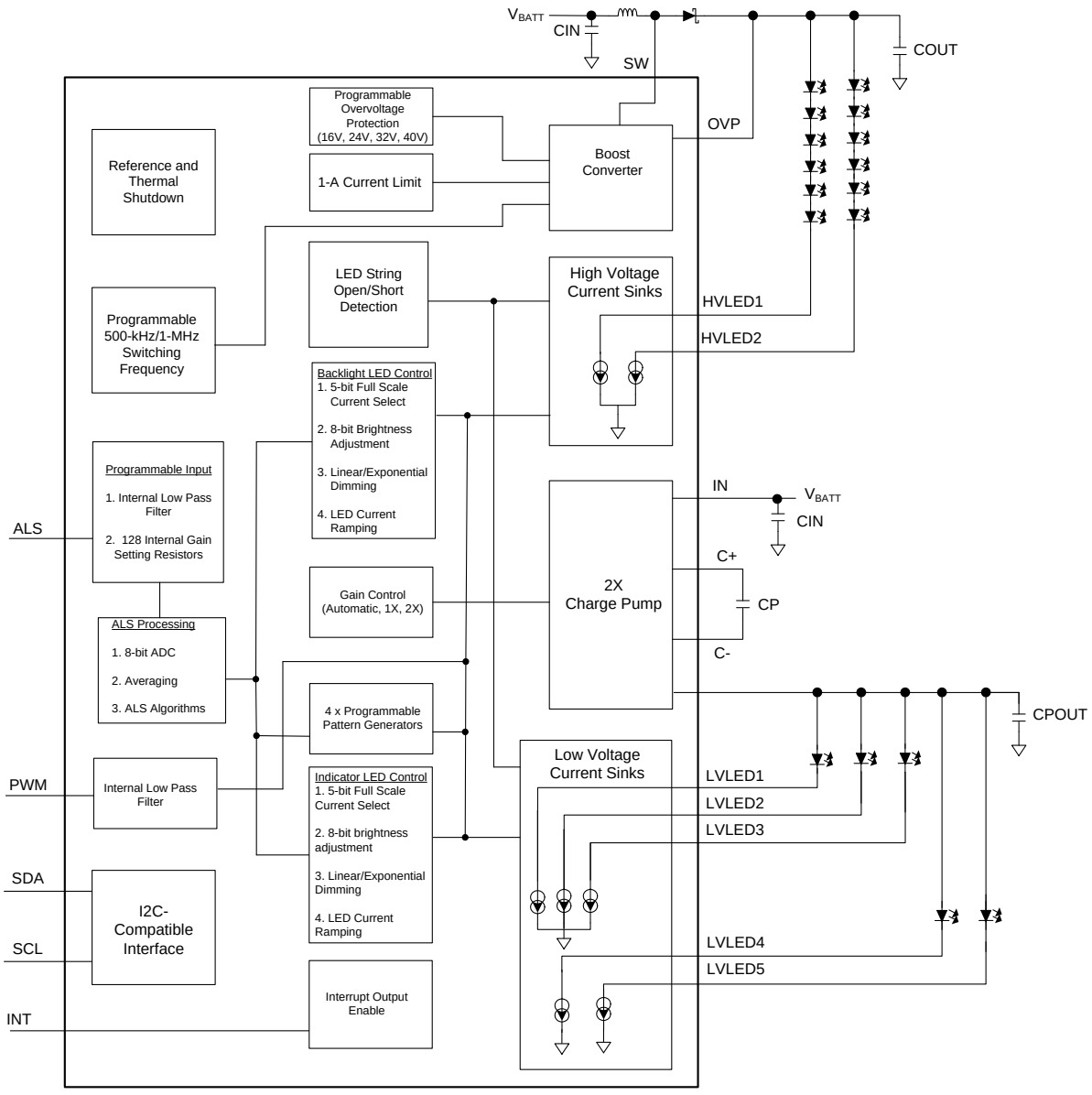
7 Detailed Description

7.1 Overview

The LM3533 provides the power for two high-voltage LED strings (up to 40 V at 30 mA each) and 5 low-voltage LEDs (up to 6 V at 30 mA each). The two high-voltage LED strings are powered from an integrated boost converter. The five low-voltage LEDs are powered from an integrated 2× charge pump.

The device is programmable over an I^2C-compatible interface. Additional features include a pulse width modulation (PWM) input for content adjustable brightness control, an ambient light sensor input (ALS) for ambient light current control, and 4 programmable pattern generators for RGB and indicator blinking functions on the low-voltage LEDs.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Control Bank Mapping

Control of the LM3533's current sinks is not done directly, but through the programming of Control Banks. The current sinks are then assigned to the programmed Control Bank. This allows for a wide variety of current control possibilities where LEDs can be grouped and controlled via specific Control Banks (see Figure 22).

7.3.1.1 High-Voltage Control Banks (A/B)

There are 2 high-voltage control banks (A and B). Both high-voltage current sinks can be assigned to either Control Bank A or Control Bank B. Assigning both current sinks to the same control bank allows for better LED current matching. Assigning each current sink to different control banks allows for each current sink to be programmed with a different current. The high-voltage control bank mapping is done via bits [1:0] of the Current Sink Output Configuration Register #1 (address 0x10).

7.3.1.2 Low-Voltage Control Banks (C, D, E, And F)

There are 4 low-voltage control banks (C, D, E, and F). Any low-voltage current sink (LVLED1 to LVLED5) can be assigned to any of the low-voltage control banks. Assigning every low-voltage current sink to the same control bank allows for the best matching between LEDs. Assigning each low-voltage current sink to different control banks allows for each current sink to be programmed with different current levels.

7.3.2 Pattern Generator

The LM3533 contains 4 independently programmable pattern generators for each Control Bank. Each pattern generator can have its own separate pattern: different rise and fall times, delays from turn-on, high and low-current settings, and pattern high and low times.

7.3.3 Ambient Light Sensor Interface

The LM3533 contains an ambient light sensor interface (ALS). The ALS input is designed to connect to the output of either an analog output or PWM output ambient light sensor. The sensor output (or ambient light information) is digitized and processed by the LM3533. The light information is then compared against the LM3533's five user-configurable brightness zones. Each brightness zone points to a brightness zone target current. Each group of target currents forms an ALS mapper. The LM3533 has three groups of ALS Mappers where each mapper can be assigned to any of the high or low-voltage control banks (see Figure 26).

7.3.4 PWM Input

The PWM input which can be assigned to any of the high- or low-voltage control banks. When assigned to a control bank, the programmed current in the control bank also becomes a function of the duty cycle at the PWM input.

7.3.5 HWEN Input

HWEN is the global hardware enable to the LM3533. HWEN must be pulled high to enable the device. HWEN is a high-impedance input so it cannot be left floating. When HWEN is pulled low the LM3533 is placed in shutdown, and all the registers are reset to their default state.

7.3.6 Thermal Shutdown

The LM3533 contains a thermal shutdown protection. In the event the die temperature reaches 140°C, the boost, charge pump and current sinks shut down until the die temperature drops to typically 125°C.

Feature Description (continued)

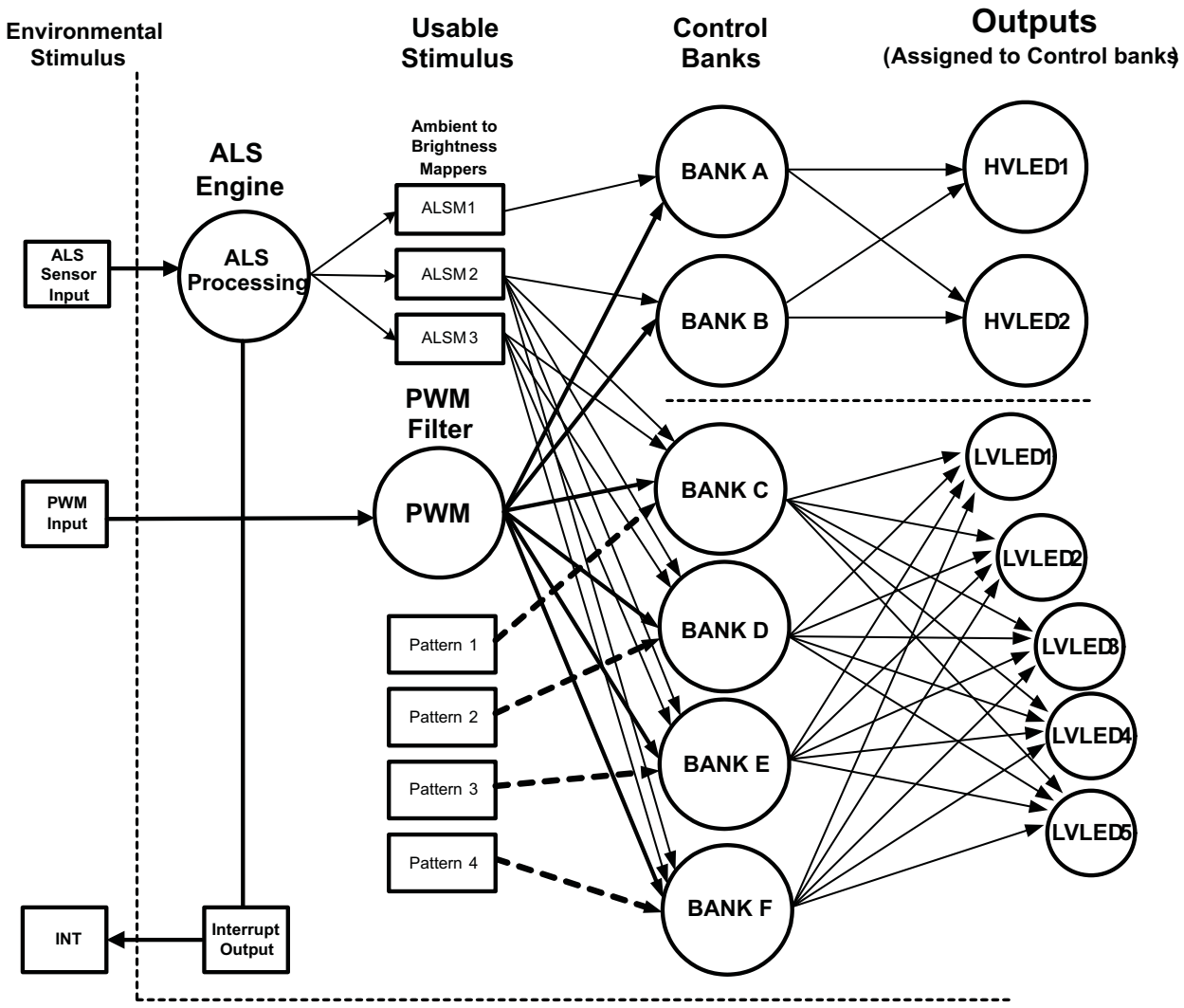


Figure 22. Functional Control Diagram

7.4 Device Functional Modes

7.4.1 High-Voltage Boost Converter

The high-voltage boost converter provides power for the two high-voltage current sinks (HVLED1 and HVLED2). The boost circuit operates using a 4.7-µH to 22-µH inductor and a 1-µF output capacitor. The selectable 500-kHz or 1-MHz switching frequency allows for the use of small external components and provides for high boost-converter efficiency. Both HVLED1 and HVLED2 feature an adaptive current regulation scheme where the feedback point (HVLED1 or HVLED2) is regulated to a minimum of 400 mV. When there are different voltage requirements in both high-voltage LED strings (string mismatch), the LM3533 regulates the feedback point of the highest voltage string to 400 mV and drop the excess voltage of the lower voltage string across the lower strings current sink.

Device Functional Modes (continued)

7.4.1.1 High-Voltage Current Sinks (HVLED1 And HVLED2)

HVLED1 and HVLED2 control the current in the high-voltage LED strings. Each current sink has 5-bit full-scale current programmability and 8-bit brightness control. Either current sink can have its current set through a dedicated brightness register or be controlled via the ambient light sensor interface. Configuration of the high-voltage current sinks is done through the Control A/B Brightness Configuration Register (see Table 8).

7.4.1.2 High-Voltage Current String Biasing

Each high-voltage current string can be powered from the LM3533's boost output (COUT) or from an external source. The Anode Connect Register bits [1:0] determine where the high-voltage current string anodes are connected. When set to 1 (default) the high-voltage current sink inputs are included in the boost feedback loop. This allows the boost converter to adjust its output voltage in order to maintain at least 400 mV at the current sink input.

When powered from alternate sources, bits [1:0] must be set to 0 . This removes the particular current sink from the boost feedback loop. In these configurations the application must ensure that the headroom voltage across the high-voltage current sink is high enough to prevent the current sink from going into dropout (see the *Typical Characteristics* for data on the high-voltage LED current vs headroom voltage).

Setting the Anode Connect Register bits also determines how the shorted high-voltage LED String Fault flag is triggered (see *Fault Flags/Protection Features*).

7.4.1.3 Boost Switching-Frequency Select

The LM3533's boost converter can have a 1-MHz or 500-kHz switching frequency. For a 500-kHz switching frequency the inductor must be between 10 µH and 22 µH. For the 1MHz switching frequency the inductor can be between 4.7 µH and 22 µH. The boost frequency is programmed through bit [1] of the OVP/Boost Frequency/PWM Polarity Select register.

7.4.2 Integrated Charge Pump

The LM3533 features an integrated (2×/1×) charge pump capable of supplying up to 150 mA. The fixed 1-MHz switching frequency allows for use of tiny 1-µF ceramic flying capacitors (CP) and output capacitor (CPOUT). The charge pump can supply the power for the low-voltage LEDs connected to LVLED1 to LVLED5 and can operate in 4 different modes: disabled, automatic gain, 1× gain, or 2× gain (see Figure 23).

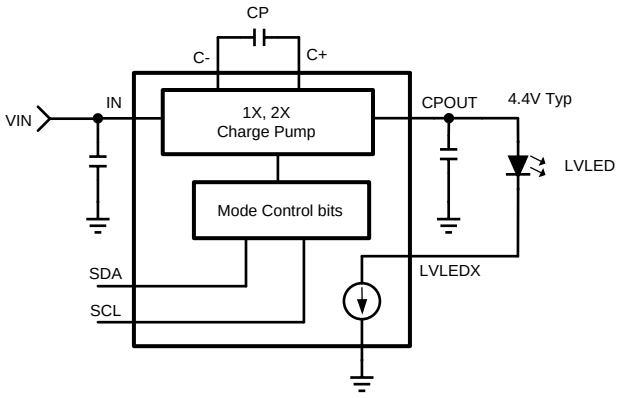


Figure 23. Integrated Charge Pump

7.4.2.1 Charge Pump Disabled

With the charge pump disabled, the path from IN to CPOUT is high impedance. Additionally, with the charge pump disabled, the low-voltage current sinks can still be active, thus allowing the low-voltage LEDs to be biased from external sources (see *Low-Voltage LED Biasing*). Disabling the charge pump also has no influence on the state of the low-voltage current sinks. For instance, if a low-voltage current string is set to have its anode connected to CPOUT, and the charge pump is disabled, the current sink continues to try to sink current.

Device Functional Modes (continued)

7.4.2.2 Automatic Gain

In Automatic Gain Mode the charge pump gain transition is actively selected to maintain LED current regulation in the CPOUT-connected, low-voltage current sinks. At higher input voltages the charge pump operates in Pass Mode (1× gain) allowing the voltage at CPOUT to track the input voltage. As V_{IN} drops, the voltage on the low-voltage current sink(s) also drops. Once any of the active, CPOUT-connected, low-voltage current sink input voltages reach typically 100 mV, the charge pump automatically switches to a gain of 2× thus preventing dropout (see *2× Gain*). Once the charge pump switches over to 2× gain it remains in 2× gain, even if the current sink input voltage goes above the switch over threshold.

7.4.2.3 Automatic Gain (Flying Capacitor Detection)

In Automatic Gain Mode the LM3533 starts up and automatically detect if there is a flying capacitor (CP) connected from C+ to C−. If there is, Automatic Gain Mode operates normally. If the detection circuitry detects that there is no flying capacitor connected, the LM3533 automatically switches to 1× Gain mode.

7.4.2.4 1× Gain

In 1× Gain Mode the charge pump passes V_{IN} directly through to CPOUT. There is a resistive drop between IN and CPOUT in this mode (1.1 Ω) which must be accounted for when determining the headroom requirement for the low-voltage current sinks. In forced 1× Gain Mode the charge pump does not switch; thus, the flying capacitor (CP) and output capacitor (CPOUT) can be omitted from the circuit.

7.4.2.5 2× Gain

In 2× Gain Mode the internal charge pump doubles V_{IN} and post-regulate CPOUT to typically 4.4 V. This allows for biasing LEDs whose forward voltages are greater than the input supply (V_{IN}).

7.4.2.6 Low-Voltage Current Sinks (LVLED1 to LVLED5)

Current sinks LVLED1 to LVLED5 each provide the current for a single LED. These low-voltage sinks are configurable with different blinking patterns via the 4 internal pattern generators. Each low-voltage current sink has 8-bit brightness control and 5-bit full-scale current programmability. Additionally, each low-voltage current sink can have its current set through a dedicated brightness register, the PWM input, the ambient light sensor interface, or a combination of these. Configuration of the low-voltage current sinks is done through the low-voltage Control Banks (C, D, E, or F). Any low-voltage current sink can be mapped to any of the low-voltage control banks.

7.4.2.7 Low-Voltage LED Biasing

Each low-voltage LED can be powered from the LM3533's charge pump output (CPOUT) or from an external source. When powered from CPOUT the anode connect bit (Anode Connect Register bits [6:2]) for that particular low-voltage current sink must be set to '1' (default). This allows for the specific low-voltage current sink to have control over the charge pumps gain control (see *Automatic Gain* section).

When powered from alternate sources (such as VIN) the anode connect bit for the particular low-voltage current sink must be set to '0'. This removes the particular current sink from the charge pump feedback loop. In these configurations the application must ensure that the headroom voltage across the low-voltage current sink is high enough to prevent the low-voltage current sinks from going into dropout (see *Typical Characteristics* for data on the low-voltage LED current vs headroom voltage).

The LVLEDx Anode Connect bits also determine how the Shorted low-voltage LED String fault flag is triggered (see *Fault Flags/Protection Features*).

7.4.3 LED Current Mapping Modes

All control banks can be programmed for either exponential or linear mapping modes (see Figure 24). These modes determine the transfer characteristic of backlight code to LED current.

Device Functional Modes (continued)

7.4.3.1 Exponential Mapping

In Exponential Mapping mode the brightness code to backlight current transfer function is given by Equation 1:

$$I_{LED} = I_{LED\_FULLSCALE} \times 0.862^{\left[46.6 - \left(\frac{Code+1}{5.5}\right)\right]} \times D_{PWM}$$

where

- $I_{LED\_FULLSCALE}$ is the full-scale LED current setting (see Table 11)
- Code is the backlight code in the Brightness register
- D_{PWM} is the PWM input duty cycle. (1)

In Exponential Mapping mode the current ramp (either up or down) appears to the human eye as a more uniform transition then the linear ramp. This is due to the logarithmic response of the eye.

7.4.3.2 Linear Mapping

In Linear Mapping Mode the brightness code to backlight current has a linear relationship and follows Equation 2:

$$I_{LED} = I_{LED\_FULLSCALE} \times \frac{1}{255} \times Code \times D_{PWM}$$

where

- $I_{LED\_FULLSCALE}$ is the full-scale LED current setting
- Code is the backlight code in the Brightness register
- D_{PWM} is the PWM input duty cycle. (2)

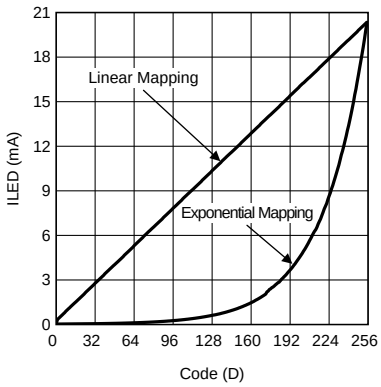


Figure 24. LED Current Mapping Modes

7.4.4 LED Current Ramping

7.4.4.1 Start-Up/Shutdown Ramp

The startup and shutdown ramp times are independently programmable in the Start-Up/Shutdown Transition Time Register (see Table 4). There are 8 different start-up and 8 different shutdown times. The start-up times can be programmed independently from the shutdown times, but teach Control bank is not independently programmable. For example, programming a start-up or shutdown time does not affect the already pre-programmed ramp time for each Control Bank.

The start-up ramp time is from when the Control Bank is enabled to when the LED current reaches its initial set point. The shutdown ramp time is from when the Control Bank is disabled to when the LED current reaches 0.

Device Functional Modes (continued)

7.4.4.2 Run-Time Ramp

Current ramping from one brightness level to the next is programmed via the Run-Time Transition Time Register (see Table 5). There are 8 different ramp-up times and 8 different ramp-down times. The ramp-up time can be programmed independently from the ramp-down time, but each Control Bank cannot be independently programmed. For example, programming a ramp-up or ramp-down time is a global setting for all Control Banks.

7.4.5 Brightness Register Current Control

For simple user-adjustable current control, the LM3533 features Brightness Register Current Control. This mode is selected via the Control Bank Brightness Configuration Registers (see Table 8 and Table 10). Once set for Brightness Register Current Control, the LED current is set by writing directly to the appropriate Control Bank Brightness Registers (see Table 28). In this mode the current for a particular Control Bank becomes a function of the full-scale LED current, the 8-bit code in the respective brightness register, and the PWM input duty cycle (if PWM is enabled). The Control Bank Brightness Register contains an 8-bit code which represents the percentage of the full-scale LED current. This percentage of full-scale current is different depending on the selected mapping mode (see *LED Current Mapping Modes*).

7.4.6 PWM Control

The LM3533 device's PWM input can be enabled for any of the Control Banks (see Table 7). Once enabled, the LED current becomes a function of the code in the Control Bank Brightness Configuration Register and the PWM input-duty cycle.

The PWM input accepts a logic level voltage and internally filters it to an analog control voltage. This results in a linear response of duty cycle to current, where 100% duty cycle corresponds to the programmed brightness code multiplied by the Full-Scale Current setting.

7.4.6.1 PWM Input Frequency Range

The usable input frequency range for the PWM input is governed on the low end by the cutoff frequency of the internal low-pass filter (540 Hz, Q = 0.33) and on the high end by the propagation delays through the internal logic. For frequencies below 2 kHz the current ripple begins to become a larger portion of the DC LED current. Additionally, at lower PWM frequencies the boost output voltage ripple increases, causing a non-linear response from the PWM duty cycle to the average LED current due to the response time of the boost. For the best response of current vs. duty cycle, the PWM input frequency must be kept between 2 kHz and 100 kHz.

7.4.6.2 PWM Input Polarity

The PWM Input can be set for active low polarity, where the LED current is a function of the negative duty cycle. This is set via the OVP/Boost Frequency/PWM Polarity Register (see Table 20).

7.4.7 ALS Current Control

The LM3533 features Ambient Light Sensor (ALS) current control which allows the LED current to be automatically set based upon the received ambient light. To implement ambient light current control the LM3533 uses a 5 brightness zone implementation with 3 sets of Zone Targets.

7.4.7.1 ALS Brightness Zones (Zone Boundaries)

The LM3533 provides for a 5 brightness zone ambient light sensor interface. This allows for the LED current in any current sink to change based upon which zone the received ambient light falls into. The brightness zones are configured via 4 ALS Zone Boundary High and 4 ALS Zone Boundary Low Registers. Each Zone Boundary register is 8 bits with a full-scale voltage of 2 V. This gives a 2 V/255 = 7.843 mV per bit. Figure 26 shows the mapping from the ALS Brightness Zone to the target backlight current.

Device Functional Modes (continued)

7.4.7.2 Zone Boundary Hysteresis

For each Zone Boundary there are two Zone Boundary Registers: a Zone Boundary High Register and a Zone Boundary Low Register (see Table 30). The difference between the Zone Boundary High and Zone Boundary Low Registers (for a specific zone) creates the hysteresis that is required to transition between zones. This hysteresis prevents the backlight current from oscillating between zones when the ALS voltage is close to a Zone Boundary Threshold. For Zone-to-Zone transitions the increasing ALS voltage must cross the Zone Boundary High Threshold in order to get into the next higher zone. Conversely, the ALS decreasing voltage must cross below the Zone Boundary Low Threshold in order to get into the next lower zone. Figure 25 describes this Zone Boundary Hysteresis.

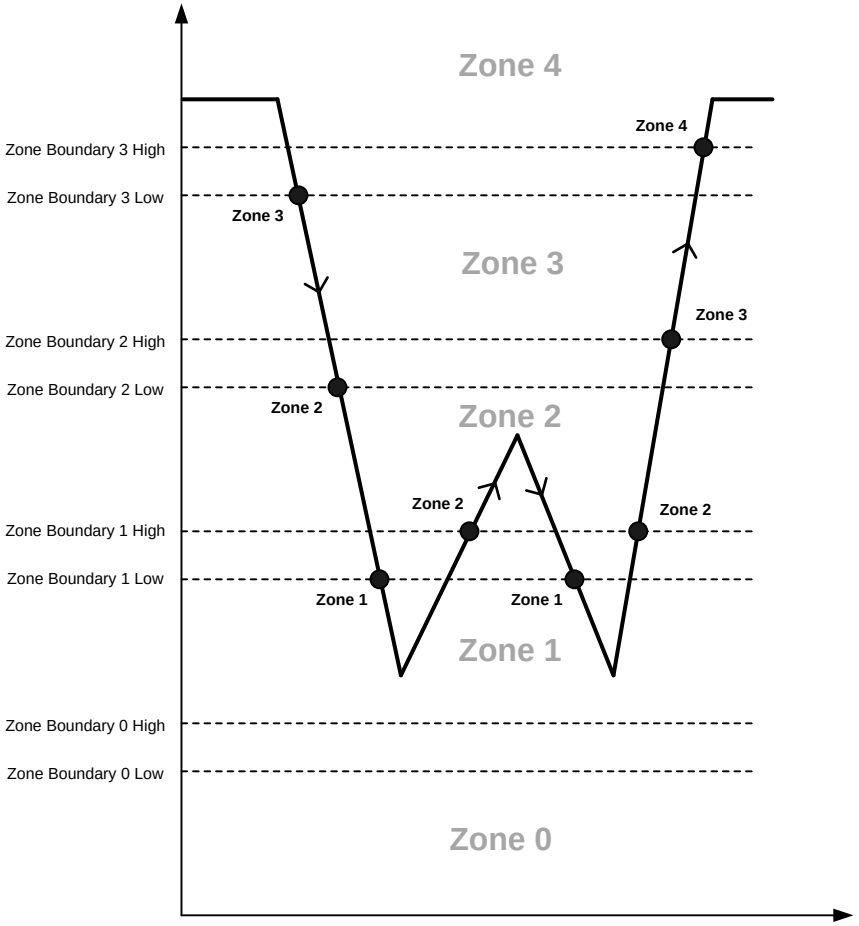


Figure 25. ALS Zone Boundary + Hysteresis

7.4.7.3 Zone Target Registers (ALSM1, ALSM2, ALSM3)

For each brightness zone there is a programmable brightness target which is set via the ALS Zone Target Registers (see Table 31, Table 32, and Table 33). There are 3 sets of ALS Zone Target Registers (ALSM1, ALSM2, and ALSM3). The ALSM1 Zone Target Registers are dedicated to only Control Bank 1. ALSM2 and ALSM3 registers can be assigned to any of the Control Banks (B – F) (see Table 8 and Table 10). Each of the Zone Target Registers consists of an 8-bit code which is a percentage of the programmed full-scale current. This percentage of full-scale current is dependent on the selected mapping mode. Figure 26 details the mapping of the ALS Brightness Zone to the ALSM_ Zone Target Registers.

Device Functional Modes (continued)

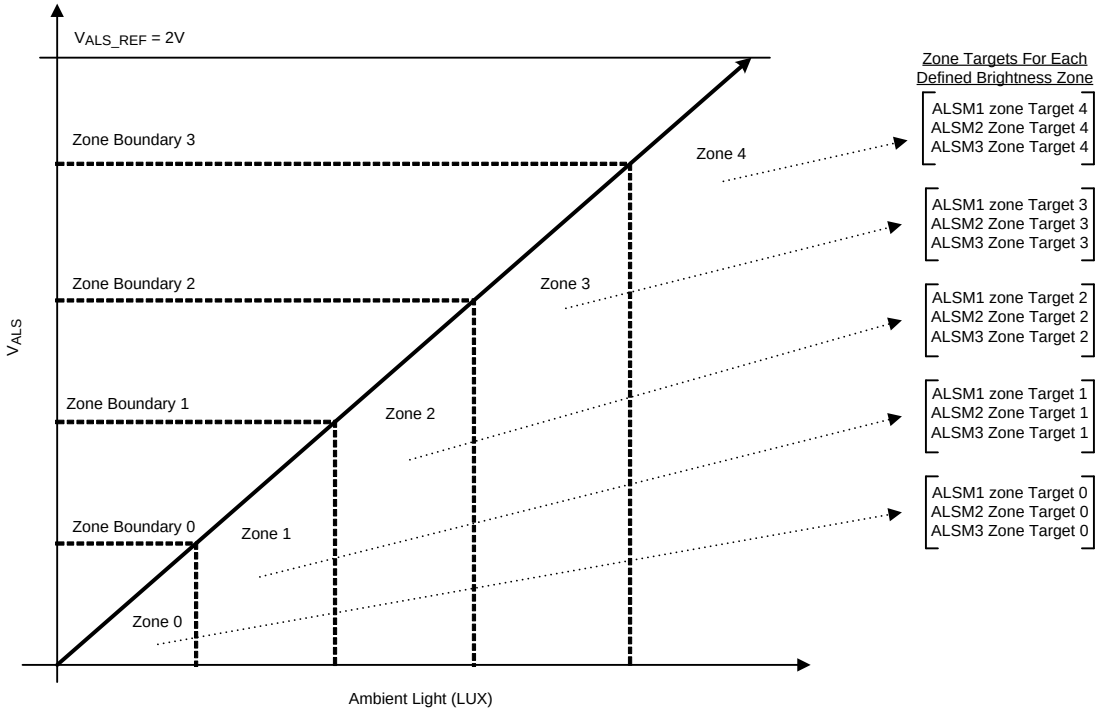


Figure 26. ALS Brightness Zone To Backlight Current Mapping

7.4.7.4 PWM Input in ALS Mode

The PWM input can be enabled for any of the 5 Brightness Zones (see Table 7). This makes the brightness target for the PWM enabled zone have its current a function of the PWM input duty cycle, the full-scale current setting for that particular bank, and the brightness target for that particular zone.

7.4.8 ALS Functional Blocks

Figure 27 shows the functional block diagram of the LM3533 device ALS interface.

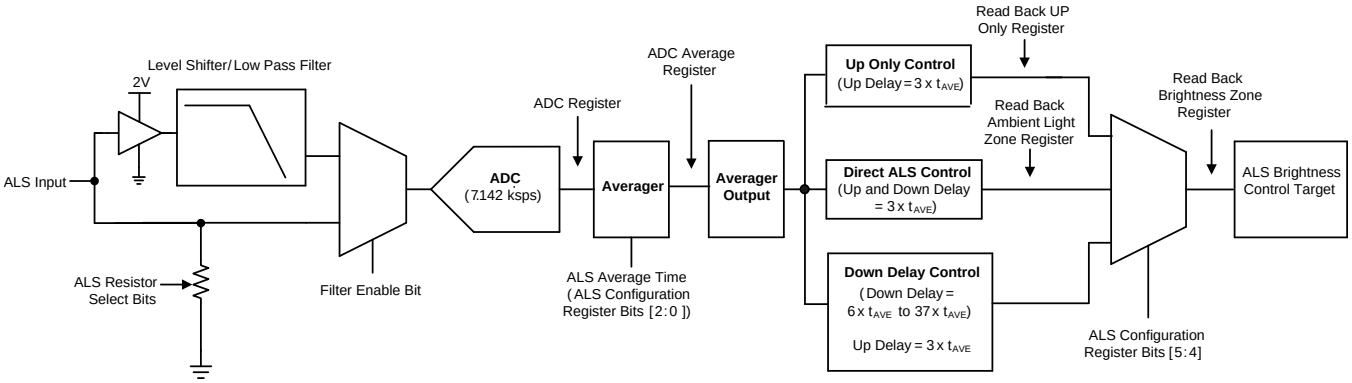


Figure 27. ALS Block Diagram

Device Functional Modes (continued)

7.4.8.1 ALS Input

The ALS input is designed to connect to an analog or PWM output ambient light sensor. The ALS Configuration Register Bit [1] selects which type of sensor interface is used at the ALS input (see Table 22).

7.4.8.2 Analog Output Ambient Light Sensors (ALS Gain Setting Resistors)

With ALS Cnfiguration Register bit [1] = 0, the ALS input is set for Analog Sensor mode. In this mode the LM3533 offers 128 programmable internal resistors at the ALS input (including a high-impedance option); see Table 21. These resistors are designed to take the output of an analog ambient light sensor and convert it into a voltage. The value of the resistor selected is typically chosen such that the ALS input voltage is 2 V at the maximum ambient light (LUX) value. The sensed voltage at the ALS input is digitized by the LM3533's internal 8-bit ADC with a full-scale value (0xFF) corresponding to 2 V.

7.4.8.3 PWM Output Ambient Light Sensors (Internal Filtering)

With the ALS Configuration Register bit [1] = 1, the ALS input is set for PWM-Sensor mode. In this mode the LM3533 offers an internal level shifter and low-pass filter (ALS PWM Input mode). With this mode enabled the ALS input accepts logic level PWM signals and converts them into a 0-to-2-V analog voltage which is then filtered. This 0-to-2-V analog representation of the PWM signal is then applied to the internal 8-bit ADC, where 2 V is the full scale (code 0xFF). The internal filter has a corner frequency of 540 Hz and provides 51 dB of attenuation (355×) at a 10-kHz input frequency.

Because the internal ADC for the ambient light sensor utilizes an 8-bit ADC, the attenuation of the ALS input signal needs to be greater than 1/255 (1 LSB = 7.843 mV) in order to realize the full 8-bit range. This forces the frequency for the PWM signal at the ALS input to be around 6 kHz or greater. For slower moving signals an external RC filter may need to be combined with the Analog Sensor Mode (see *Application and Implementation*).

When the ALS input is set for ALS PWM Input Mode the internal ALS resistor setting is automatically set for high impedance, no matter what the setting in the ALS Select Register.

7.4.8.4 Internal 8-Bit ADC

The LM3533 digitizes the ALS voltage using an internal 8-bit ADC. The ADC is active as long as the ALS enable bit is set. Once set, the ADC begins sampling and converting the voltage at the ALS input at 7.142 ksps. The ADC output can be read back via the ADC register (address 0x37). With the ALS enable bit set, the ADC register is updated every 140 µs. Figure 28 details the timing of the ADC.

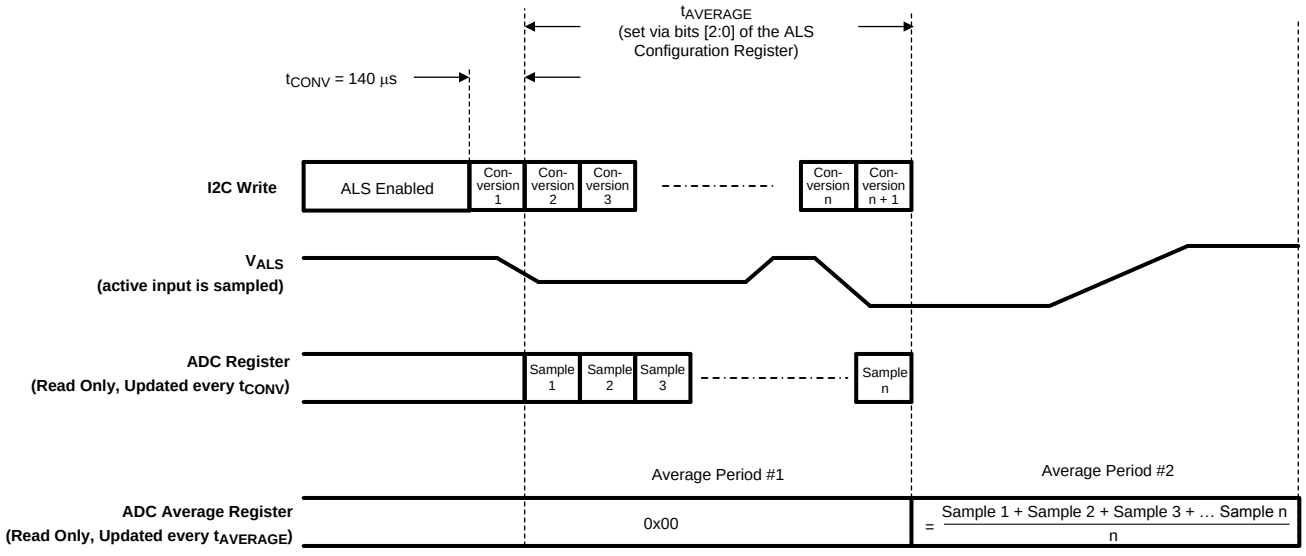


Figure 28. ADC Timing

Device Functional Modes (continued)

7.4.8.5 ALS Averager

Once digitized the output of the ADC is sent into the ALS averager. The averager computes the average of the number of samples taken over the programmed average period. The ALS average times are set via bits [5:3] in the ALS Configuration Register. The output of the ALS average can be read back via the ADC Average register (address 0x38). With the ALS Enable bit set, the ADC Average register is updated after each average period (see Figure 28). After every average period the Averager Output stores the information for which brightness zone the ALS input voltage resides in (see Figure 27).

7.4.8.6 Initializing the ALS

On initial start-up of the ALS Interface, the Ambient Light Zone defaults to Zone 0. This allows the ALS to start off in a predictable state. The drawback is that Zone 0 is often not representative of the true ALS Brightness Zone, as the ALS input can get to its ambient light representative voltage much faster than the LED current is allowed to change. In order to avoid a multiple average time wait for the backlight current to get to its correct state, the LM3533 switches over to a fast average period (1.1 ms) during the ALS start-up. This quickly brings the ALS Brightness Zone (and the backlight current) to its correct setting (see Figure 29).

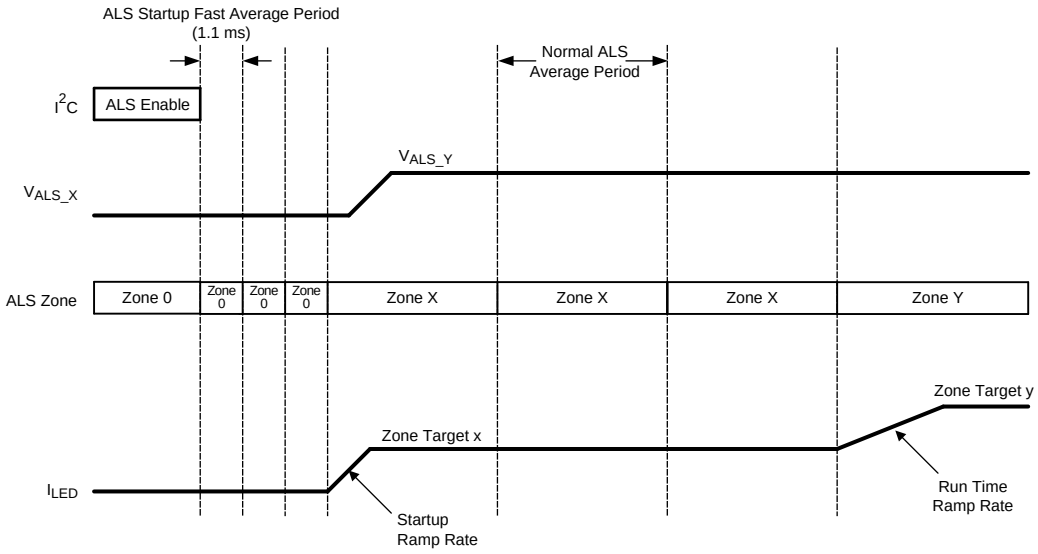


Figure 29. ALS Start-up Sequence

7.4.8.7 ALS Algorithms

There are three ALS algorithms that can be selected independently by each ALS Mapper (ALSM1, ALSM2, and ALSM3) (see Table 23). The ALS algorithms are: direct, up only, and down delay.

7.4.8.8 ALS Rules

For each algorithm, the ALS follows these basic rules:

1. For the ALS Interface to force a change in the backlight current (to a higher zone target), the averager output must have shown an increase for 3 consecutive average periods, or an increase and a remain at the new zone for 3 consecutive average periods.
2. For the ALS Interface to force a change in the backlight current (to a lower zone target), the averager output must have shown a decrease for 3 consecutive average periods, or a decrease and remain at the new zone for 3 consecutive average periods.
3. If condition 1 or 2 above is satisfied, and during the next average period the averager output changes again in the same direction as the last change, the LED current immediately changes at the beginning of the next average period.

Device Functional Modes (continued)

4. If condition 1 or 2 above is satisfied, and the next average period shows no change in the average zone, or shows a change in the opposite direction, then the criteria in condition 1 or 2 must be satisfied again before the ALS interface can force a change in the backlight current.
5. The Averager Output (see Figure 27) contains the zone that is determined from the most recent full average period.
6. The ALS Interface only forces a change in the backlight current at the beginning of an average period.
7. When the ALS forces a change in the backlight current the change is to the brightness target pointed to by the zone in the Averager Output.

7.4.8.9 Direct ALS Control

In direct ALS control the LM3533 ALS Interface can force the backlight current to either a higher zone target or a lower zone target using the rules described in *ALS Rules*. In the example of Figure 30, the plot shows the ALS voltage, the current average zone which is the zone determined by averaging the ALS voltage in the current average period, the Averager Output which is the zone determined from the previous full average period, and the target backlight current that is controlled by the ALS Interface. The following steps detail the Direct ALS algorithm:

1. When the ALS is enabled the ALS fast start-up (1.1-ms average period) quickly brings the Averager Output to the correct zone. This takes 3 fast average periods or approximately 3.3ms.
2. The 1st average period the ALS voltage averages to Zone 4.
3. The 2nd average period the ALS voltage averages to Zone 3.
4. The 3rd average period the ALS voltage averages to Zone 0 and the Averager Output shows a change from Zone 4 to Zone 3.
5. The 4th average period the ALS voltage averages to Zone 2 and the Averager Output remains at its changed state of Zone 3.
6. The 5th average period the ALS voltage averages to Zone 1. The Averager Output shows a change from Zone 3 to Zone 2. Because this is the 3rd average period that the Averager Output has shown a change in the decreasing direction from the initial Zone 4, the backlight current is forced to change to the current Averager Output (Zone 2's) target current.
7. The 6th average period the ALS voltage averages to Zone 2. The Averager Output changes from Zone 2 to Zone 1. Because this is in the same direction as the previous change, the backlight current is forced to change to the current Averager Output (Zone 1's) target current.
8. The 7th average period the ALS voltage averages to Zone 3. The Averager Output changes from Zone 1 to Zone 2. Because this change is in the opposite direction from the previous change, the backlight current remains at Zone 1's target.
9. The 8th average period the ALS voltage averages to Zone 3. The Averager Output changes from Zone 2 to Zone 3.
10. The 9th average period the ALS voltage averages to Zone 3. The Averager Output remains at Zone 3. Because this is the 3rd average period that the Averager Output has shown a change in the increasing direction from the initial Zone 1, the backlight current is forced to change to the current Averager Output (Zone 3's) target current.
11. The 10th average period the ALS voltage averages to Zone 4. The Averager Output remains at Zone 3.
12. The 11th average period the ALS voltage averages to Zone 4. The Averager Output changes to Zone 4.
13. The 12th average period the ALS voltage averages to Zone 4. The Averager Output remains at Zone 4.
14. The 13th average period the ALS voltage averages to Zone 4. The Averager Output remains at Zone 4. Because this is the 3rd average period that the Averager Output has shown a change in the increasing direction from the initial Zone 3, the backlight current is forced to change to the current Averager Output (Zone 4's) target current.

Device Functional Modes (continued)

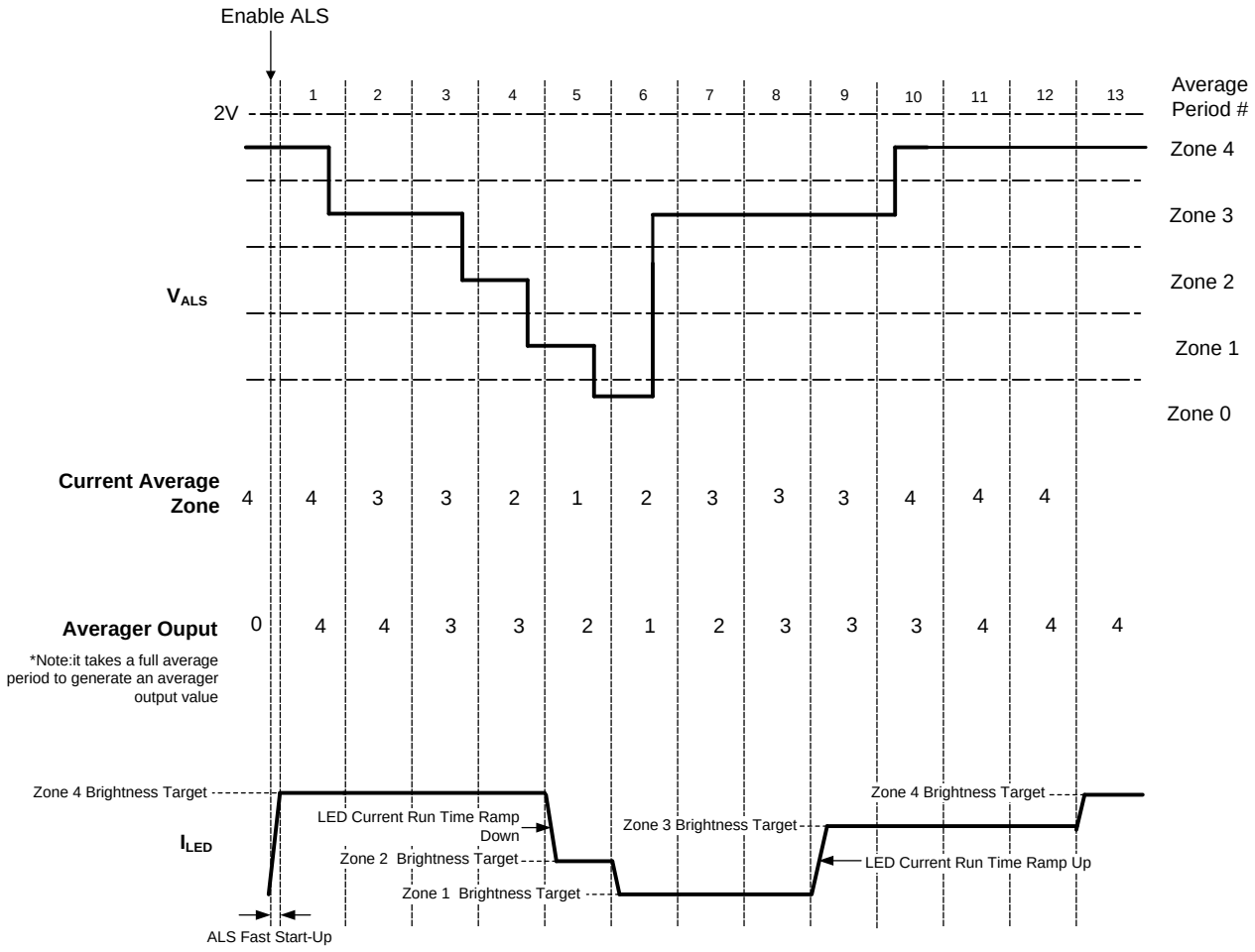


Figure 30. Direct ALS Control

7.4.8.10 Up-Only Control

The ALS Up-Only Control algorithm is similar to Direct ALS Control except the ALS Interface can only program the backlight current to a higher zone target. Referring to Figure 31:

1. When the ALS is enabled the ALS fast startup (1.1ms average period) quickly brings the Averager Output to the correct zone. This takes 3 fast average periods or approximately 3.3 ms.
2. The 1st average period the ALS voltage averages to Zone 1.
3. The 2nd average period the ALS voltage averages to Zone 0.
4. The 3rd average period the ALS voltage averages to Zone 0, and the Averager Output shows a change from Zone 1 to Zone 0.
5. The 4th average period the ALS voltage averages to Zone 2, and the Averager Output remains at its changed state of Zone 0.
6. The 5th average period the ALS voltage averages to Zone 2. The Averager Output remains at Zone 0. Because the Up Only algorithm is chosen the backlight current remains at the Zone 1 target even though this is the 3rd consecutive average period that the Averager Output has shown a change since the initial Zone 1.
7. The 6th average period the ALS voltage averages to Zone 2. The Averager Output changes from Zone 0 to Zone 2.
8. The 7th average period the ALS voltage averages to Zone 3. The Averager Output remains at Zone 2.
9. The 8th average period the ALS voltage averages to Zone 3. The Averager Output remains at Zone 2.

Device Functional Modes (continued)

Because this is the 3rd average period that the Averager Output has shown a change in the up direction, the backlight current is forced to change to the current Averager Output (Zone 2's) target current.

10. The 9th average period the ALS voltage averages to Zone 3. The Averager Output changes from Zone 2 to Zone 3. Because this is a change in the increasing Zone direction, and is a consecutive change following a new backlight target current transition, the backlight current is again forced to change to the current Averager Output (Zone 3's) target current.
11. The 10th average period the ALS voltage averages to Zone 4. The Averager Output remains at Zone 3.
12. The 11th average period the ALS voltage averages to Zone 4. The Averager Output changes to Zone 4.
13. The 12th average period the ALS voltage averages to Zone 4. The Averager Output remains at Zone 4.
14. The 13th average period the ALS voltage averages to Zone 4. The Averager Output remains at Zone 4. Because this is the 3rd average period that the Averager Output has shown a change in the increasing direction from the initial Zone 3, the backlight current is forced to change to the current Averager Output (Zone 4's) target current.

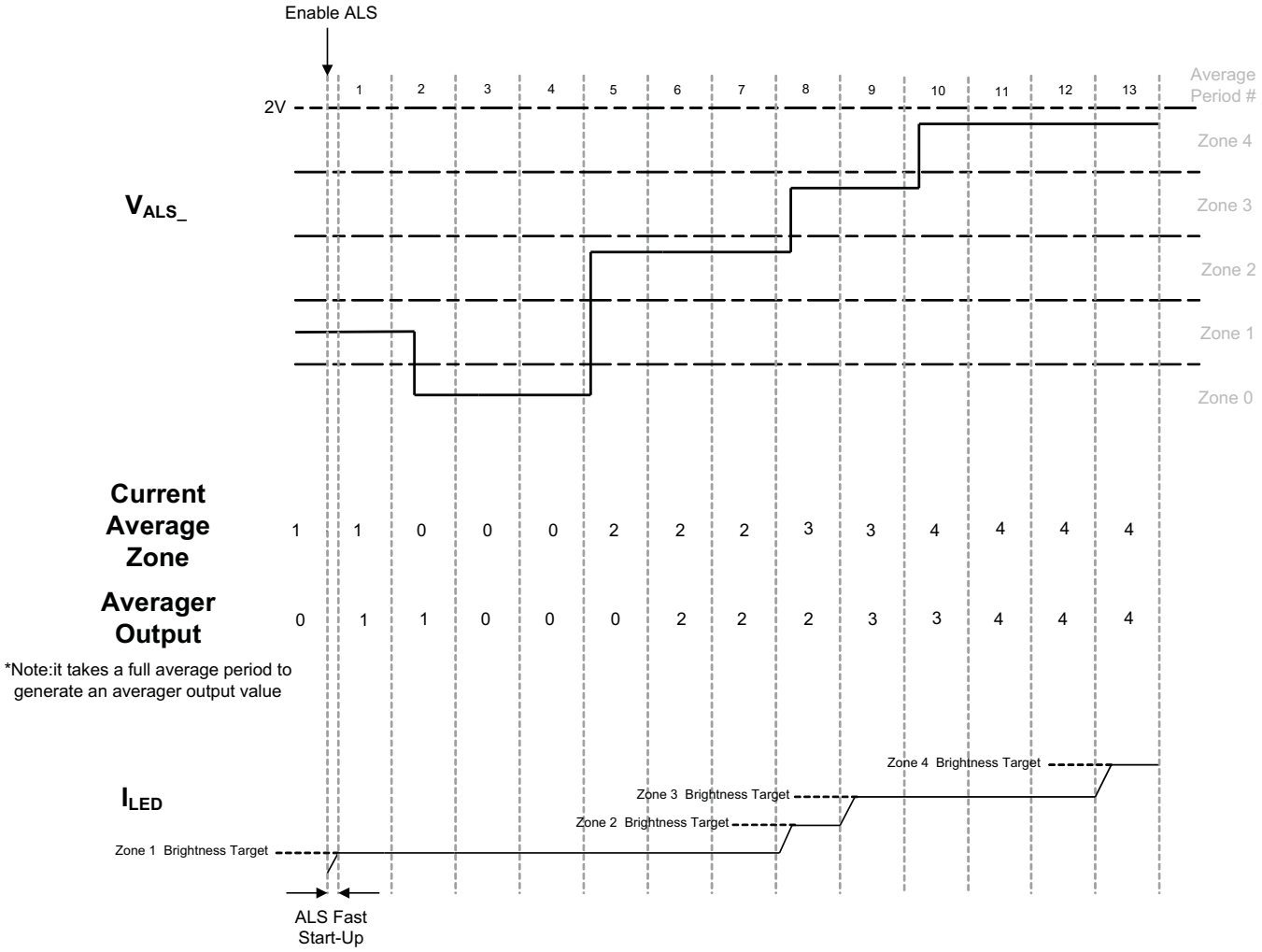


Figure 31. ALS Up-Only Control

Device Functional Modes (continued)

7.4.8.11 Down-Delay Control

The Down-Delay algorithm uses all the same rules from *ALS Rules*, except it provides for adding additional average period delays required for decreasing transitions of the Averager Output, before the LED current is programmed to a lower zone target current. The additional average period delays are programmed via the ALS Down Delay register. The register provides 32 settings for increasing the down delay from 3 extra (code 00000) up to 34 extra (code 11111). For example, if the down delay algorithm is enabled, and the ALS Down Delay register was programmed with 0x00 (3 extra delays), then the Averager Output would need to see 6 consecutive changes in decreasing Zones (or 6 consecutive average periods that changed and remained lower), before the backlight current was programmed to the lower zones target current. Referring to Figure 32, assume that Down Delay is enabled, and the ALS Down Delay register is programmed with 0x02 (5 extra delays, or 8 average period total delays for downward changes in the backlight target current):

1. When the ALS is enabled the ALS fast startup (1.1ms average period) quickly brings the Averager Output to the correct zone. This takes 3 fast average periods or approximately 3.3 ms.
2. The first average period the ALS voltage averages to Zone 3.
3. The second average period the ALS voltage averages to Zone 2. The Averager Output remains at Zone 3.
4. The 3rd through 7th average period the ALS voltage averages to Zone 2, and the Averager Output stays at Zone 2.
5. The 8th average period the ALS voltage averages to Zone 4. The Averager Output remains at Zone 2.
6. The 9th and 10th average periods the ALS voltage averages to Zone 4. The Averager Output is at Zone 4. Because the Averager Output increased from Zone 2 to Zone 4 and the required Down Delay time was not met (8 average periods), the backlight current was never changed to the Zone 2's target current.
7. The 11th average period the ALS voltage averages to Zone 2. The Averager Output remains at Zone 4. Because this is the 3rd consecutive average period where the Averager Output has shown a change (increasing direction) since the change from Zone 2, the backlight current transitions to Zone 4's target current.
8. The 12th through 26th average periods the ALS voltage averages to Zone 2. The Averager Output remains at Zone 2. At the start of average period #19 the Averager Output has shown the required 8 average period delay from the initial change from Zone 4 to Zone 2. As a result the backlight current is programmed to Zone 2's target current.

Device Functional Modes (continued)

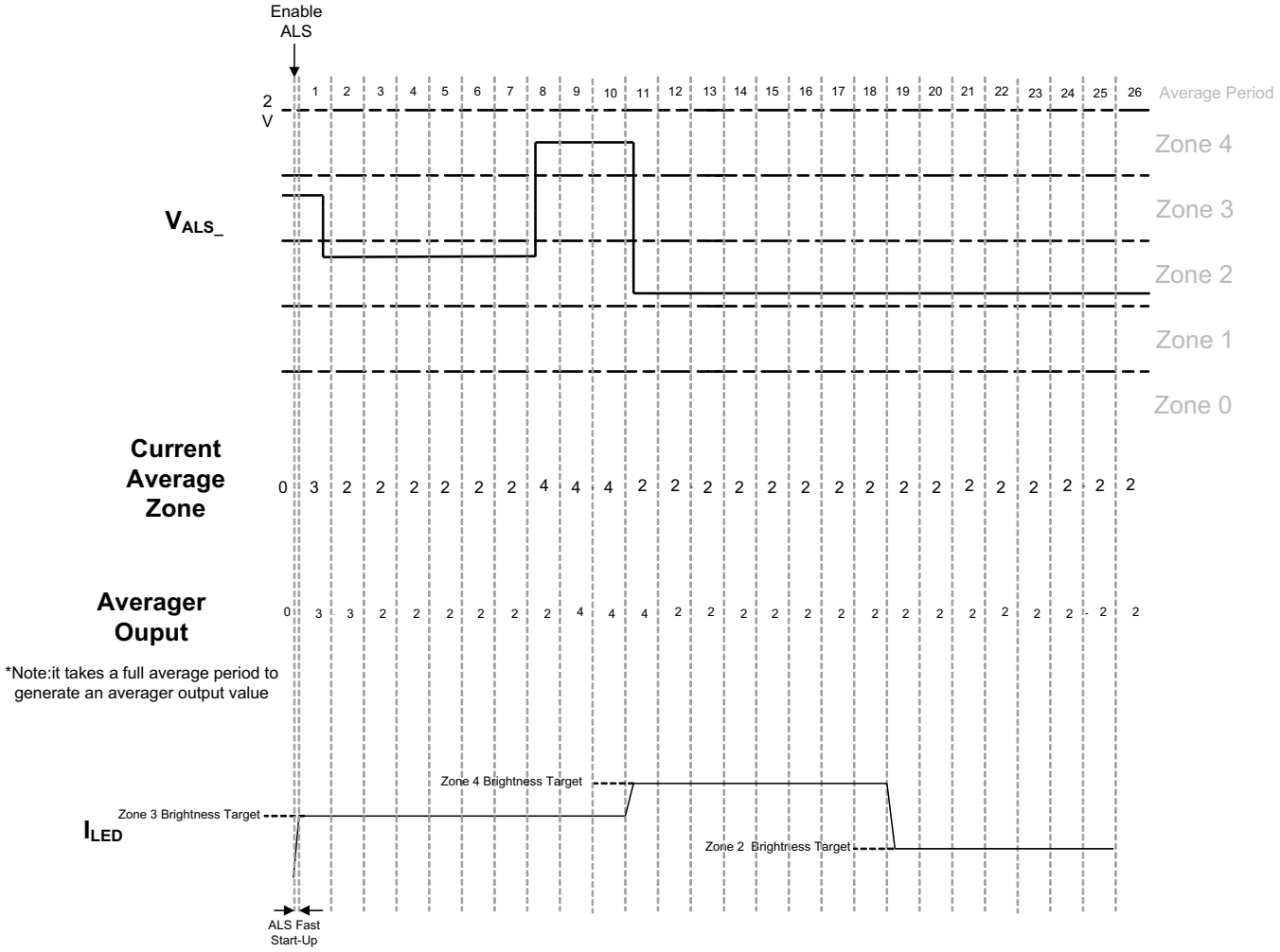


Figure 32. ALS Down-Delay Control

7.4.9 Pattern Generator

The LM3533 contains 4 programmable pattern generators (one for each low-voltage control bank). Each pattern generator has the ability to drive a unique programmable pattern. Each pattern generator has its own set of registers available for pattern programming. The programmable patterns are : delay time, rise time, fall time, high period, low period, high current and low current (see Figure 33).

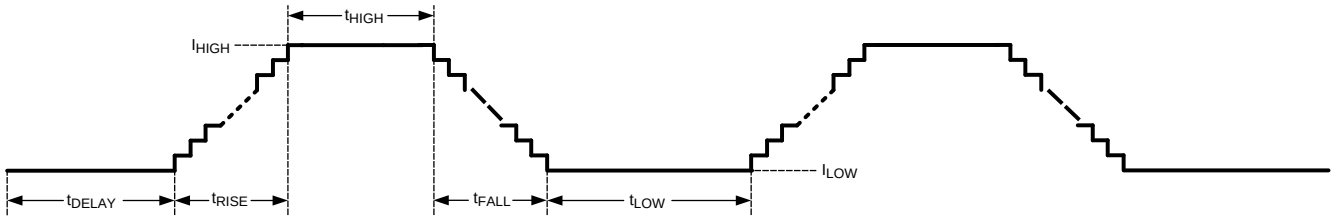


Figure 33. Pattern Generator Timing

Device Functional Modes (continued)

7.4.9.1 Delay Time

The Delay time (t_{DELAY}) is the delay from when the pattern is enabled to when the LED current begins ramping up in the control bank's assigned current source(s). The pattern starts when bit [3] of the respective Control Bank Brightness Configuration Register is written high. There is one t_{DELAY} register for each pattern generator (4 total). The selectable times are programmed with the lower 6 bits of the t_{DELAY} registers. The times are split into 2 groups where codes 0x00 to 0x3C are short durations from 16.384 ms (code 0x00) up to 999.424 ms (code 0x3C) or 16.384 ms/bit. The higher codes (0x3D to 0x7F) select t_{DELAY} from 1130.496 ms up to 9781.248 ms, or 131.072 ms/bit (see Table 35).

7.4.9.2 Rise Time

The LED current rise time (t_{RISE}) is the time the LED current takes to move from the low-current brightness level (I_{LOW}) to the high-current brightness level (I_{HIGH}). The rise time of the LED current (t_{RISE}) is set via the Pattern Generator Rise Time Registers. Each Pattern Generator has its own rise-time register. There are 8 available rise-time settings (see Table 42).

7.4.9.3 Fall Time

The LED current fall time (t_{FALL}) is the time the LED current takes to move from the high-current brightness level (I_{HIGH}) to the low-current brightness level (I_{LOW}). The fall time of the LED current (t_{FALL}) is set via the Pattern Generator Fall Time Registers. Each Pattern Generator has its own fall-time register. There are 8 available fall-time settings (see Table 43).

7.4.9.4 High Period

The LED current high period (t_{HIGH}) is the duration that the LED pattern spends at the high LED current set point (t_{HIGH}). The t_{HIGH} times are programmed via the Pattern Generator t_{HIGH} Registers. The programmable times are broken into 2 groups. The first set (from code 0x00 to 0x3C) increases the t_{HIGH} time in steps of 16.384 ms. The second set (from code 0x3D to 0x7F) increases the t_{HIGH} time in steps of 131.072 ms (see Table 39).

7.4.9.5 Low Period

The LED current low period (t_{LOW}) is the duration that the LED current spends at the low LED current set point (I_{LOW}). The t_{LOW} times are programmed via one of the Pattern Generator t_{LOW} Registers. There are 256 t_{LOW} settings and are broken into 3 groups of linearly increasing times. The first set (from code 0x00 to 0x3C) increases the t_{LOW} time in steps of 16.384ms. The second set (from code 0x3D to 0x7F) increases the t_{LOW} time in steps of 131.072 ms. The third set (from code 0x80 to 0xFF) increases the t_{LOW} time in steps of 524.288 ms (see Table 37).

7.4.9.6 Low-Level Brightness

The LED current low brightness level (I_{LOW}) is the LED current set point that the pattern rests at during the t_{LOW} period. This level is set via the Pattern Generator Low Level Brightness Register(s). The brightness level has 8 bits of programmability. I_{LOW} is a function of the Control Banks full-scale Current setting, the code in the Pattern Generator Low-Level Brightness Register, the Mapping Mode selected, and the PWM input duty cycle (if PWM is enabled).

For exponential mapping I_{LOW} is:

$$I_{LOW} = I_{LED\_FULLSCALE} \times 0.85^{\left[40 - \left(\frac{BREGL\_X+1}{6.4}\right)\right]} \times D_{PWM} \quad (3)$$

For linear mapping I_{LOW} is:

$$I_{LOW} = I_{LED\_FULLSCALE} \times \frac{1}{255} \times BREGL\_X \times D_{PWM} \quad (4)$$

BREGL_X is the Pattern Generator Low-Level Brightness Register setting for the specific Control Bank (see Table 40).

Device Functional Modes (continued)

7.4.9.7 High-Level Brightness

The LED current high brightness level (I_{HIGH}) is the LED current set point that the pattern rests at during the t_{HIGH} period. This high-current level is set via the Control Banks Brightness Register (BREGCH to BREGFH). The brightness level has 8 bits of programmability. I_{HIGH} is a function of the Control Banks Full-Scale Current setting, the code in the Control Banks Brightness Register, the Mapping Mode selected, and the PWM input duty cycle (if PWM is enabled).

For exponential mapping I_{HIGH} is:

$$I_{LED} = I_{LED\_FULLSCALE} \times 0.862^{\left[46.6 - \left(\frac{Code+1}{5.5}\right)\right]} \times D_{PWM} \quad (5)$$

For linear mapping I_{HIGH} is:

$$I_{HIGH} = I_{LED\_FULLSCALE} \times \frac{1}{255} \times BREGH\_X \times D_{PWM} \quad (6)$$

BREGH_X is the Control Banks Brightness Register setting for the specific Control Bank (see Table 28).

7.4.9.8 ALS Controlled Pattern Current

The current levels (I_{HIGH} and I_{LOW}) of the programmable pattern can also be influenced by the ALS input. All the same ALS algorithms apply to the pattern generator current levels (Direct, Up Only, and Down Delay). The difference, however, for the ALS Controlled Pattern Current is that the pattern current is not changed to zone-defined brightness targets, but is changed by a scaled factor of the existing I_{HIGH} and I_{LOW} levels. These scaled factors are programmable in the ALS Pattern Scaler Registers (see Table 17, Table 18, and Table 19). Each defined brightness zone has a 4-bit (16-level) scale factor, which takes the programmed pattern current code and multiplies it by the programmed scale factor. This produce a new I_{HIGH} and I_{LOW} current level ranging from 1/16 × BREGH and 1/16 × BREGL up to 16/16 × BREGH and 16/16 × BREGL for each ALS zone (see Figure 34). There is only one set of scale factors for all the pattern generators.

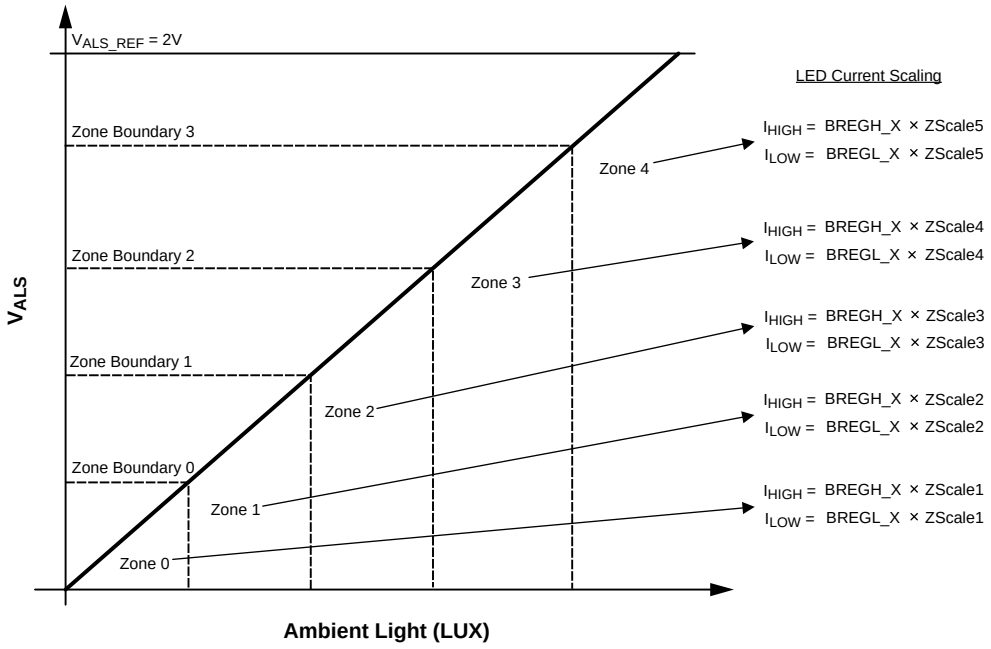


Figure 34. ALS Controlled Pattern Current Scaling

Device Functional Modes (continued)

For low-voltage control banks that do not have their pattern generator enabled, ALS current control is done via the ALS Mappers. Once a pattern generator is enabled, that particular Control Bank then uses the pattern scalers for ALS Current Control.

7.4.9.9 Interrupt Output Mode

When INT Mode is enabled (ALS Zone Information Register Bit [0] = 1), INT pin is configured as an interrupt output. INT is an open-drain output with an active pulldown of typically 66 Ω. In INT Mode the INT output pulls low if the ALS interface is enabled, and the ALS input has changed zones. Reading back the ALS Zone Information while in this mode clears the INT output and reset it to its open-drain state.

7.4.10 Fault Flags/Protection Features

The LM3533 contains both an LED open and LED short fault detection. These fault detections are designed to be used in production level testing and not normal operation. For the fault flags to operate, they must be enabled via the LED Fault Enable Register (see Table 47).

7.4.10.1 Open LED String (HVLED)

An open LED string is detected when the voltage at the input to any active high-voltage current sink has fallen below 200 mV, and the boost output voltage has hit the OVP threshold. This test assumes that the HVLED string that is being detected for an open is connected to the LM3533 boost output (COUT+) (see Table 13). For an HVLED string not connected to the LM3533 boost output voltage, but connected to another voltage source, the boost output will not trigger the OVP flag. In this case an open LED string is not detected.

The procedure for detecting an open fault in the HVLED current sinks (provided they are connected to the boost output voltage) is:

- Apply power to the LM3533
- Enable Open Fault (Register 0xB2, bit [0] = 1)
- Configure HVLED1 and HVLED2 for LED string anode connected to COUT (Register 0x25, bits[1:0] = (1,1)
- Set Bank A full-scale current to 20.2 mA (Register 0x1F = 0x13)
- Set Bank A brightness to max (Register 0x40 = 0xFF)
- Set the startup ramp times to the fastest setting (Register 0x12 = 0x00)
- Assign HVLED1 and HVLED2 to Bank A (Register 0x10, Bits [1:0] = (0, 0)
- Enable Bank A (Register 0x27 Bit[0] = 1
- Wait 4ms
- Read back bits[1:0] of register 0xB0. Bit [0] = 1 (HVLED1 open). Bit [1] = 1 (HVLED2 open)
- Disable all banks (Register 0x27 = 0x00)

7.4.10.2 Shorted LED String (HVLED)

The LM3533 features an LED short fault flag indicating one or more of the HVLED strings have experienced a short. The method for detecting a shorted HVLED strings is if the current sink is enabled and the string voltage (V_{OUT} – $V_{HVLED1/2}$) falls to below (V_{IN} – 1 V). This test must be performed on one HVLED string at a time. Performing the test with both current sinks enabled can result in a faulty reading if one of the strings is shorted and the other is not.

The procedure for detecting a short in an HVLED string is:

- Apply power to the LM3533
- Enable Short Fault (Register 0xB2, bit [1] = 1)
- Enable Feedback on the HVLED Current Sinks (Register 0x25 = 0xFF)
- Set Bank A full-scale current to 20.2 mA (Register 0x1F = 0x13)
- Set Bank A brightness to max (Register 0x40 = 0xFF)
- Set the startup ramp times to the fastest setting (Register 0x12 = 0x00)
- Assign HVLED1 to Bank A (Register 0x10, Bits [1:0] = (1, 0)
- Enable Bank A (Register 0x27 Bit[0] = 1
- Wait 4 ms

Device Functional Modes (continued)

- Read back bits[0] of register 0xB1. 1 = HVLED1 open
- Disable all banks (Register 0x27 = 0x00)
- Repeat the procedure for the HVLED2 string

7.4.10.3 Open LED (LVLED)

The LM3533 features an open LED fault flag indicating one or more of the active LVLED strings are open. An open in an LVLED string is flagged if the voltage at the input to any active low-voltage current sink goes below 110 mV.

Because the open LED detect is flagged when any active current sink input falls below 110 mV, certain configurations can result in falsely triggering an open. These include:

1. LED anode tied to CPOUT, charge pump in 1× gain, and VIN drops low enough to bring any active LVLED current sink below 110 mV.
2. LED anode not tied to CPOUT and VLED_ANODE goes low enough to bring any active LVLED current sink below 110 mV.

The following list describes a test procedure that can be used in detecting an open in the LVLED strings:

- Apply power to the LM3533
- Enable Open Fault (Register 0xB2, bit [0] = 1)
- Configure all LVLED strings for Anode connected to CPOUT (register 0x25 bits[6:2] = 1)
- Force the Charge Pump into 2× gain (Register 0x26 Bits[2:1] = 11). Ensure that CPOUT and CP are in the circuit and that (V_{CPOUT} is > VF_{LVLED} + V_{HR_LV})
- Set Bank C full-scale Current to 20.2 mA (Register 0x21 = 0x13)
- Set Bank C brightness to max (Register 0x42 = 0xFF)
- Set the startup ramp times to the fastest setting (Register 0x12 = 0x00)
- Assign LVLED1 - LVLED5 to Bank C (Register 0x11 = 0x00, Register 0x10 = 0x00)
- Enable Bank C (Register 0x27 Bit[2] = 1
- Wait 4ms
- Read back bits[6:2] of register 0xB0. 1 indicates an open and a 0 indicates normal operation (see Table 45).
- Disable all banks (Register 0x27 = 0x00)

7.4.10.4 Shorted LED (LVLED)

The LM3533 features an LED short fault flag indicating when any active low-voltage LED is shorted (anode to cathode). A short in an LVLED is determined when the LED voltage (V_{CPOUT} – V_{HR}) falls below 1 V.

A procedure for determining a short in an LVLED string is:

- Apply Power
- Enable Short Fault (Register 0xB2, bit [1] = 1)
- Enable Feedback on the LVLED Current Sinks (Register 0x25 = 0xFF)
- Set Bank C full-scale current to 20.2 mA (Register 0x21 = 0x13)
- Set Bank C brightness to max (Register 0x42 = 0xFF)
- Set the startup ramp times to the fastest setting (Register 0x12 = 0x00)
- Assign LVLED1 to LVLED5 to Bank C (Register 0x11 = 0x00, Register 0x10 = 0x00)
- Set Charge Pump to 1× gain (Register 0x26 = 0x40)
- Enable Bank C (Register 0x27 Bit[2] = 1
- Wait 4ms
- Read bits[6:2] from register 0xB1. A 1 indicates short, and a 0 indicates normal (see Table 46).
- Disable all banks (Register 0x27 = 0x00)

Device Functional Modes (continued)

7.4.10.5 Overvoltage Protection (Inductive Boost)

The overvoltage protection threshold (OVP) on the LM3533 has 4 different programmable options (16 V, 24 V, 32 V, and 40 V). The OVP protects the device and associated circuitry from high voltages in the event the high-voltage LED string becomes open. During normal operation, the LM3533 inductive boost converter boosts the output up so as to maintain at least 400 mV at the active, high-voltage (C_{OUT} connected) current sink inputs. When a high-voltage LED string becomes open, the feedback mechanism is broken, and the boost converter overboosts the output. When the output voltage reaches the OVP threshold the boost converter stops switching, thus allowing the output node to discharge. When the output discharges to V_{OVP} – 1 V the boost converter begins switching again. The OVP sense is at the OVP pin, so this pin must be connected directly to the inductive boost output capacitor's positive terminal.

For high-voltage current sinks that have the Anode Connect Register setting such that the high-voltage current sinks anodes are not connected to COUT (feedback is disabled), the over-voltage sense mechanism is not in place to protect the input to the high-voltage current sink. In this situation the application must ensure that the voltage at HVLED1 or HVLED2 doesn't exceed 40 V.

The default setting for OVP is set at 16 V. For applications that require higher than 16 V at the boost output, the OVP threshold must be programmed to a higher level after powerup.

7.4.10.6 Current Limit (Inductive Boost)

The NMOS switch current limit for the LM3533 inductive boost is set at 1 A. When the current through the LM3533 NFET switch hits this overcurrent protection threshold (OCP), the device turns the NFET off and the inductor's energy is discharged into the output capacitor. Switching is then resumed at the next cycle. The current limit protection circuitry can operate continuously each switching cycle. The result is that during high-output power conditions the device can continuously run in current limit. Under these conditions the LM3533's inductive boost converter stops regulating the headroom voltage across the high-voltage current sinks. This results in a drop in the LED current.

7.4.10.7 Current Limit (Charge Pump)

The LM3533 charge pump's output current limit is set high enough so that the device supports 29.8 mA (maximim full-scale current) in all LVLED current sinks. This would typically be (29.5 mA × 5 = 149 mA. For 1× gain the output current limit is typically 350 mA (V_{IN} = 3.6 V). For 2× gain the current limit is typically 240 mA (output referred), with a typical limit on the input current of 480 mA. The *Typical Characteristics* detail the charge pump current limit vs V_{IN} at both 1× and 2× gain settings (see *Typical Characteristics*).

7.5 Programming

7.5.1 I²C-Compatible Interface

7.5.1.1 Start and Stop Conditions

The LM3533 is controlled via an I²C-compatible interface. START and STOP conditions classify the beginning and the end of the I²C session. A START condition is defined as SDA transitioning from HIGH to LOW while SCL is HIGH. A STOP condition is defined as SDA transitioning from LOW to HIGH while SCL is HIGH. The I²C master always generates START and STOP conditions. The I²C bus is considered busy after a START condition and free after a STOP condition. During data transmission the I²C master can generate repeated START conditions. A START and a repeated START condition are equivalent function-wise. The data on SDA must be stable during the HIGH period of the clock signal (SCL). In other words, the state of SDA can only be changed when SCL is LOW.

Programming (continued)

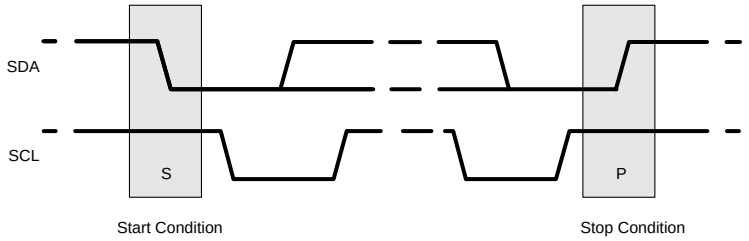


Figure 35. Start and Stop Sequences

7.5.1.2 I²C-Compatible Address

The chip address for the LM3533 is 0110110 (36h) for the -40 device and 0111000 (38h) for the -40A device. After the START condition, the I^2C master sends the 7-bit chip address followed by an eighth read or write bit (R/W). R/W= 0 indicates a WRITE and R/W = 1 indicates a READ. The second byte following the chip address selects the register address to which the data is written. The third byte contains the data for the selected register.

7.5.1.3 Transferring Data

Every byte on the SDA line must be eight bits long, with the most significant bit (MSB) transferred first. Each byte of data must be followed by an acknowledge bit (ACK). The acknowledge related clock pulse (9th clock pulse) is generated by the master. The master releases SDA (HIGH) during the 9th clock pulse. The LM3533 pulls down SDA during the 9th clock pulse signifying an acknowledge. An acknowledge is generated after each byte has been received.

Table 1 lists the available registers within the LM3533.

7.6 Register Maps

7.6.1 LM3533 Register Descriptions

Table 1. LM3533 Register Definitions

Name	Address	Power On Reset
Current Sink Output Configuration 1	0x10	0x92
Current Sink Output Configuration 2	0x11	0x0F
Start Up/Shut Down Ramp Rates	0x12	0x00
Run Time Ramp Rates	0x13	0x00
Control Bank A PWM Configuration	0x14	0x38
Control Bank B PWM Configuration	0x15	0x38
Control Bank C PWM Configuration	0x16	0x38
Control Bank D PWM Configuration	0x17	0x38
Control Bank E PWM Configuration	0x18	0x38
Control Bank F PWM Configuration	0x19	0x38
Control Bank A/B Brightness Configuration	0x1A	0x00
Control Bank C Brightness Configuration	0x1B	0x00
Control Bank D Brightness Configuration	0x1C	0x00
Control Bank E Brightness Configuration	0x1D	0x00
Control Bank F Brightness Configuration	0x1E	0x00
Control Bank A Full-Scale Current	0x1F	0x13
Control Bank B Full-Scale Current	0x20	0x13
Control Bank C Full-Scale Current	0x21	0x13
Control Bank D Full-Scale Current	0x22	0x13
Control Bank E Full-Scale Current	0x23	0x13

Register Maps (continued)

Table 1. LM3533 Register Definitions (continued)

Name	Address	Power On Reset
Control Bank F Full-Scale Current	0x24	0x13
Anode Connect	0x25	0x7F
Charge Pump Control	0x26	0x00
Control Bank Enable	0x27	0x00
Pattern Generator Enable/ALS Scaling Control	0x28	0x00
ALS Pattern Scaler #1(Zones 5, 4)	0x29	0xFF
ALS Pattern Scaler #2 (Zones 3, 2)	0x2A	0xFF
ALS Pattern Scaler #3 (Zone 1)	0x2B	0xF0
OVP/Frequency/PWM Polarity	0x2C	0x08
R_ALS Select	0x30	0x00
ALS Configuration	0x31	0x20
ALS Algorithm Select	0x32	0x00
ALS Down Delay Control	0x33	0x00
Read-Back ALS Zone	0x34	0x00
Read-Back Down Delay ALS Zone	0x35	0x00
Read-Back Up Only ALS Zone	0x36	0x00
Read-Back ADC	0x37	0x00
Read-Back Average ADC	0x38	0x00
Brightness Register A	0x40	0x00
Brightness Register B	0x41	0x00
Brightness Register C	0x42	0x00
Brightness Register D	0x43	0x00
Brightness Register E	0x44	0x00
Brightness Register F	0x45	0x00
ALS Zone Boundary 0 High	0x50	0x35
ALS Zone Boundary 0 Low	0x51	0x33
ALS Zone Boundary 1 High	0x52	0x6A
ALS Zone Boundary 1 Low	0x53	0x66
ALS Zone Boundary 2 High	0x54	0xA1
ALS Zone Boundary 2 Low	0x55	0x99
ALS Zone Boundary 3 High	0x56	0xDC
ALS Zone Boundary 3 Low	0x57	0xCC
ALS M1 Zone Target 0	0x60	0x33
ALS M1 Zone Target 1	0x61	0x66
ALS M1 Zone Target 2	0x62	0x99
ALS M1 Zone Target 3	0x63	0xCC
ALS M1 Zone Target 4	0x64	0xFF
ALS M2 Zone Target 0	0x65	0x33
ALS M2 Zone Target 1	0x66	0x66
ALS M2 Zone Target 2	0x67	0x99
ALS M2 Zone Target 3	0x68	0xCC
ALS M2 Zone Target 4	0x69	0xFF
ALS M3 Zone Target 0	0x6A	0x33
ALS M3 Zone Target 1	0x6B	0x66
ALS M3 Zone Target 2	0x6C	0x99
ALS M3 Zone Target 3	0x6D	0xCC

Register Maps (continued)

Table 1. LM3533 Register Definitions (continued)

Name	Address	Power On Reset
ALS M3 Zone Target 4	0x6E	0xFF
Pattern Generator 1 Delay	0x70	0x00
Pattern Generator 1 Low Time	0x71	0x00
Pattern Generator 1 High Time	0x72	0x00
Pattern Generator 1 Low Level Brightness	0x73	0x00
Pattern Generator 1 Rise Time	0x74	0x00
Pattern Generator 1 Fall Time	0x75	0x00
Pattern Generator 2 Delay	0x80	0x00
Pattern Generator 2 Low Time	0x81	0x00
Pattern Generator 2 High Time	0x82	0x00
Pattern Generator 2 Low Level Brightness	0x83	0x00
Pattern Generator 2 Rise Time	0x84	0x00
Pattern Generator 2 Fall Time	0x85	0x00
Pattern Generator 3 Delay	0x90	0x00
Pattern Generator 3 Low Time	0x91	0x00
Pattern Generator 3 High Time	0x92	0x00
Pattern Generator 3 Low Level Brightness	0x93	0x00
Pattern Generator 3 Rise Time	0x94	0x00
Pattern Generator 3 Fall Time	0x95	0x00
Pattern Generator 4 Delay	0xA0	0x00
Pattern Generator 4 Low Time	0xA1	0x00
Pattern Generator 4 High Time	0xA2	0x00
Pattern Generator 4 Low Level Brightness	0xA3	0x00
Pattern Generator 4 Rise Time	0xA4	0x00
Pattern Generator 4 Fall Time	0xA5	0x00
LED Open Fault Read Back	0xB0	0x00
LED Short Fault Read Back	0xB1	0x00
LED Fault Enables	0xB2	0x00

Table 2. Output Configuration Register 1 (Address 0x10)

Bit [7:6] LVLED3 Configuration	Bits [5:4] LVLED2 Configuration	Bits [3:2] LVLED1 Configuration	Bit [1] HVLED2 Configuration	Bit 0 HVLED1 Configuration
00 = LVLED3 is controlled by Control Bank C	00 = LVLED2 is controlled by Control Bank C	00 = LVLED1 is controlled by Control Bank C **(Default)**	0 = HVLED2 is controlled by Control Bank A	0 = HVLED1 is controlled by Control Bank A **(Default)**
01 = LVLED3 is controlled by Control Bank D	01 = LVLED2 is controlled by Control Bank D **(Default)**	01 = LVLED1 is controlled by Control Bank D	1 = HVLED2 is controlled by Control Bank B **(Default)**	1 = HVLED1 is controlled by Control Bank B
10 = LVLED3 is controlled by Control Bank E **(Default)**	10 = LVLED2 is controlled by Control Bank E	10 = LVLED1 is controlled by Control Bank E		
11 = LVLED3 is controlled by Control Bank F	11 = LVLED2 is controlled by Control Bank F	11 = LVLED1 is controlled by Control Bank F		

Table 3. Output Configuration Register 2 (Address 0x11)

Bits [7:4] Not used	Bits [3:2] LVLED5 Configuration	Bits [1:0] LVLED4 Configuration
	00 = LVLED5 is controlled by Control Bank C	00 = LVLED4 is controlled by Control Bank C
	01 = LVLED5 is controlled by Control Bank D	01 = LVLED4 is controlled by Control Bank D
	10 = LVLED5 is controlled by Control Bank E	10 = LVLED4 is controlled by Control Bank E
	11 = LVLED5 is controlled by Control Bank F **(Default)**	11 = LVLED4 is controlled by Control Bank F **(Default)**

Table 4. LED Current Start-Up/Shutdown Transition Time Register (Address 0x12)

Bits [7:6]	Bits [5:3] Startup Transition Time	Bits [2:0] Shutdown Transition Time
Not Used	000 = 2048µs **(Default)** 001 = 262ms 010 = 524ms 011 = 1.049s 100 =2.097s 101 = 4.194s 110 = 8.389s 111 = 16.78s Startup time is from when the device is enabled via I^2C to when the initial target current is reached.	000 = 2048µs **(Default)** 001 = 262ms 010 = 524ms 011 = 1.049s 100 =2.097s 101 = 4.194s 110 = 8.389s 111 = 16.78s Shutdown ramp time is from when the device is shutdown via I^2C until the current sink ramps to 0.

Table 5. LED Current Run-Time Transition Time Register (Address 0x13)

Bits [7:6]	Bits [5:3] Transition Time Ramp Up	Bits [2:0] Transition Time Ramp Down
Not Used	000 = 2048µs **(Default)** 001 = 262ms 010 = 524ms 011 = 1.049s 100 =2.097s 101 = 4.194s 110 = 8.389s 111 = 16.78s	000 = 2048µs **(Default)** 001 = 262ms 010 = 524ms 011 = 1.049s 100 =2.097s 101 = 4.194s 110 = 8.389s 111 = 16.78s

Table 6. Control Bank PWM Configuration Registers (Addresses 0x14 to 0x19)

Address	Function
0x14	Control Bank A PWM Configuration Register
0x15	Control Bank B PWM Configuration Register
0x16	Control Bank C PWM Configuration Register
0x17	Control Bank D PWM Configuration Register
0x18	Control Bank E PWM Configuration Register
0x19	Control Bank F PWM Configuration Register

Table 7. Control Bank PWM Configuration Register Bit Settings

[Bit 7:6] Not Used	Bit 5 Zone 4 PWM Enabled	Bit 4 Zone 3 PWM Enabled	Bit 3 Zone 2 PWM Enabled	Bit 2 Zone 1 PWM Enabled	Bit 1 Zone 0 PWM Enabled	Bit 0 PWM Enabled
	0 = PWM input is disabled in Zone 4	0 = PWM input is disabled in Zone 3	0 = PWM input is disabled in Zone 2	0 = PWM input is disabled in Zone 1 **(Default)**	0 = PWM input is disabled in Zone 0 **(Default)**	0 = PWM Input is disabled **(Default)**
	1 = PWM input is enabled in Zone 4 **(Default)**	1 = PWM input is enabled in Zone 3 **(Default)**	1 = PWM input is enabled in Zone 2 **(Default)**	1 = PWM input is enabled in Zone 1	1 = PWM input is enabled in Zone 0	1 = PWM Input is enabled

Table 8. Control Bank A/B Brightness Configuration Register (Address 0x1A)

Bits [7:4] Not Used	Bit 3 Control Bank B Mapping Mode	Bit 2 BREGB/ALSM2 Control	Bit 1 Control Bank A Mapping Mode	Bit 0 BREGA/ALSM1 Control
	0 = Exponential Mapping **(Default)**	0 = Control Bank B is configured for Brightness Register Current Control **(Default)**	0 = Exponential Mapping **(Default)**	0 = Control Bank A is configured for Brightness Register Current Control **(Default)**
	1 = Linear Mapping	1 = Control Bank B is configured for ALS current control via the ALSM2 Zone Target Registers	1 = Linear Mapping	1 = Control Bank A is configured for ALS current control via the ALSM1 Zone Target Registers

Table 9. Low-Voltage Control Bank Brightness Configuration Registers (Addresses 0x1B, 0x1C, 0x1D, 0x1E)

Address	Function
0x1B	Control Bank C Brightness Configuration Register
0x1C	Control Bank D Brightness Configuration Register
0x1D	Control Bank E Brightness Configuration Register
0x1E	Control Bank F Brightness Configuration Register

Table 10. Low-Voltage Control Bank Brightness Configuration Register Bit Settings

Bits [7:4] Not Used	Bit 3 Pattern Generator Enable	Bit 2 Mapping Mode	Bits [1:0] Current Control
	0 = Pattern Generator is disabled for Control Bank_ **(Default)**	0 = Exponential Mapping **(Default)**	0X = Control Bank_ is configured for Brightness Register Current Control via the respective Brightness Register **(Default)**
	1 = Pattern Generator is enabled for Control Bank_	1 = Linear Mapping	10 = Control Bank_ is configured for ALS current control via the ALSM2 Zone Target Registers
			11 = Control Bank_ is configured for ALS current control via the ALSM3 Zone Target Registers

Table 11. Control Bank Full-Scale Current Registers (Addresses 0x1F, 0x20, 0x21, 0x22, 0x23, 0x24)

Address	Function
0x1F	Control Bank A Full-Scale Current Register
0x20	Control Bank B Full-Scale Current Register
0x21	Control Bank C Full-Scale Current Register
0x22	Control Bank D Full-Scale Current Register
0x23	Control Bank E Full-Scale Current Register
0x24	Control Bank F Full-Scale Current Register

Table 12. Control Bank Full-Scale Current Register Bit Settings

Bits [7:5] Not Used	Bits [4:0] Control A Full-Scale Current Select Bits
N/A	00000 = 5mA
	:
	:
	10011 = 20.2mA **(Default)**
	:
	:
	11111 = 29.8mA The full-scale Current vs code is given by Equation 7: $I_{LED\_FULLSCALE}$ = 5 mA + Code × 0.8 mA (7)

Table 13. Anode Connect Register (Address 0x25)

Bits [7] Not Used	Bit 6 LVLED5 Anode Connect	Bit 5 LVLED4 Anode Connec	Bit 4 LVLED3 Anode Connect	Bit 3 LVLED2 Anode Connect	Bit 2 LVLED1 Anode Connect	Bit 1 HVLED2 Anode Connect	Bit 0 HVLED1 Anode Connect
	0 = LVLED5 LED anode is not connected to CPOUT	0 = LVLED4 LED anode is not connected to CPOUT	0 = LVLED3 LED anode is not connected to CPOUT	0 = LVLED2 LED anode is not connected to CPOUT	0 = LVLED1 LED anode is not connected to CPOUT	0 = HVLED2 LED string anode is not connected to COUT	0 = HVLED1 LED string anode is not connected to COUT
	1 = LVLED5 LED anode is connected to CPOUT **(Default)**	1 = LVLED4 LED anode is connected to CPOUT **(Default)**	1 = LVLED3 LED anode is connected to CPOUT **(Default)**	1 = LVLED2 LED anode is connected to CPOUT **(Default)**	1 = LVLED1 LED anode is connected to CPOUT **(Default)**	1 = HVLED2 LED string anode is connected to COUT **(Default)**	1 = HVLED1 LED string anode is connected to COUT **(Default)**

Table 14. Charge Pump Control Register (Address 0x26)

Bits [7:3] Not Used	Bits [2:1] Gain Select	Bit 0 Charge Pump Disable
N/A	0X = Automatic gain select **(Default)** 10 = Gain set at 1x 11 = Gain set at 2x	0 = Charge pump enabled **(Default)** 1 = Charge pump disabled; charge pump is high impedance from IN to CPOUT.

Table 15. Control Bank Enable Register (Address 0x27)

Bits [7:6] Not Used	Bit 5 Control F Enable	Bit 4 Control E Enable	Bit 3 Control D Enable	Bit 2 Control C Enable	Bit 1 Control B Enable	Bit 0 Control A Enable
	0 = Control Bank F is disabled **(Default)**	0 = Control Bank E is disabled **(Default)**	0 = Control Bank D is disabled **(Default)**	0 = Control Bank C is disabled **(Default)**	0 = Control Bank B is disabled **(Default)**	0 = Control Bank A is disabled **(Default)**
	1 = Control Bank F is enabled	1 = Control Bank E is enabled	1 = Control Bank D is enabled	1 = Control Bank C is enabled	1 = Control Bank B is enabled	1 = Control Bank A is enabled

Table 16. Pattern Generator Enable/ALS Scaling Control (Address 0x28)

Bit 7 Pattern 4 ALS Scaling Enable	Bit 6 Pattern 4 Enable	Bit 5 Pattern 3 ALS Scaling Enable	Bit 4 Pattern 3 Enable	Bit 3 Pattern 2 ALS Scaling Enable	Bit 2 Pattern 2 Enable	Bit 1 Pattern 1 ALS Scaling Enable	Bit 0 Pattern 1 Enable
0 = Pattern 4 Scaling Disabled **(Default)**	0 = Pattern 4 Disabled **(Default)**	0 = Pattern 3 Scaling Disabled **(Default)**	0 = Pattern 3 Disabled **(Default)**	0 = Pattern 2 Scaling Disabled **(Default)**	0 = Pattern 2 Disabled **(Default)**	0 = Pattern 1 Scaling Disabled **(Default)**	0 = Pattern 1 Disabled **(Default)**

Table 16. Pattern Generator Enable/ALS Scaling Control (Address 0x28) (continued)

Bit 7 Pattern 4 ALS Scaling Enable	Bit 6 Pattern 4 Enable	Bit 5 Pattern 3 ALS Scaling Enable	Bit 4 Pattern 3 Enable	Bit 3 Pattern 2 ALS Scaling Enable	Bit 2 Pattern 2 Enable	Bit 1 Pattern 1 ALS Scaling Enable	Bit 0 Pattern 1 Enable
1 = Pattern 4 Scaling Enabled	1 = Pattern 4 Enabled	1 = Pattern 3 Scaling Enabled	1 = Pattern 3 Enabled	1 = Pattern 2 Scaling Enabled	1 = Pattern 2 Enabled	1 = Pattern 1 Scaling Enabled	1 = Pattern 1 Enabled

Note: If a low-voltage control bank is set to receive its brightness information from either ALSM2 or ALSM3, and then a pattern generator is enabled for that Control Bank, the Control Bank ignores the ALSM2 or ALSM3 zone target information. This prevents conflicts from ALSM2/ALSM3 zone targets and ALS controlled pattern currents.

Table 17. ALS Zone Pattern Scaler 1 (Address 0x29)

Bits [7:4] ALS Pattern Scaler (Zone 4)	Bits [3:0] ALS Pattern Scaler (Zone 3)
0000 = 1/16	0000 = 1/16
0001 = 2/16	0001 = 2/16
:	:
1111 = 16/16 **(Default)**	1111 = 16/16 **(Default)**

Table 18. ALS Zone Pattern Scaler 2 (Address 0x2A)

Bits [7:4] ALS Pattern Scaler (Zone 2)	Bits [3:0] ALS Pattern Scaler (Zone 1)
0000 = 1/16	0000 = 1/16
0001 = 2/16	0001 = 2/16
:	:
1111 = 16/16 **(Default)**	1111 = 16/16h **(Default)**

Table 19. ALS Zone Pattern Scaler 3 (Address 0x2B)

Bits [7:4] Not Used	Bits [3:0] ALS Pattern Scaler (Zone 0)
	0000 = 1/16 **(Default)**
	0001 = 2/16
	:
	1111 = 16/16

Table 20. OVP/Boost Frequency/PWM Polarity Select (Address 0x2C)

Bits [7:4] Not Used	Bit 3 PWM Polarity	Bit [2:1] Boost OVP Select	Bit 1 Boost Frequency Select
	0 = Active Low Polarity 1 = Active High Polarity **(Default)**	00 = 16V **(Default)** 01 = 24V 10 = 32V 11 = 40V	0 = 500 kHz **(Default)** 1 = 1MHz

Table 21. R_ALS Select Register (Address 0x30)

Bit 7 Not Used	Bits [6:0] ALS Resistor Select Code
	0000000 = ALS input is high impedance **(Default)**
	0000001 = 200kΩ (10µA at 2V full-scale)
	0000010 = 100kΩ (20µA at 2V full-scale)
	:
	:
	:
	1111110 = 1.587kΩ (1.26mA at 2V full-scale)
	1111111 = 1.575kΩ (1.27mA at 2V full-scale)

The selectable codes are available which give a linear step in currents of 10 µA per code based upon 2V/R_ALS. This gives a code to resistance relationship of:

$$R_{ALS} = \frac{2V}{10\ \mu A\ x\ Code(D)} \quad (8)$$

Table 22. ALS Configuration Register (Address 0x31)

Bit [7:6] Not Used	Bits [5:3] ALS Average Times	Bit 2 Fast startup Enable/Disable	Bit 1 ALS Input Mode	Bit 0 ALS Enable/Disable
	000 = 17.92 ms 001 = 35.84ms 010 = 71.68ms 011 = 143.36ms 100 = 286.72ms **(Default)** 101 = 573.44ms 110 = 1146.88ms 111 = 2293.76ms	0 = ALS fast startup is enabled **(Default)** 1 = ALS fast startup is disabled	0 = ALS is set for Analog Sensor Input Mode **(Default)** 1 = ALS is set for PWM Sensor Input Mode	0 = ALS is disabled **(Default)** 1 = ALS is enabled

Table 23. ALS Algorithm Select Register (Address 0x32)

Bits [7:6] ALS Pattern Generator Zone Algorithm Select	Bits [5:4] ALSM3 zone Algorithm Select	Bits [3:2] ALSM2 zone Algorithm Select	Bits [1:0] ALSM1 zone Algorithm Select
00 = Direct Control **(Default)**	00 = Direct Control **(Default)**	00 = Direct Control **(Default)**(Default)	00 = Direct Control (default)
01 = Up Only Control	01 = Up Only Control	01 = Up Only	01 = Up Only
1× = Down Delay Control	1× = Down Delay Control	1X = Down Delay	1× = Down Delay

Table 24. ALS Down Delay Control Register (Address 0x33)

Bits [7:4] Not Used	Bits [4:0] Down Delay Settings (# Indicates total average periods required to force a change in the down direction)
	00000 = 6 **(Default)**
	:
	:
	:
	11111 = 37

Table 25. ALS Zone Information Register (Address 0x34)

Bits [7:5] Not Used	Bits [4:2] Average Zone Information Bits	Bit 1 Zone Change Bit	Bit 0 Interrupt Enable Bit
	000 = Zone 0 **(Default)** 001 = Zone 1 010 = Zone 2 011 = Zone 3 1XX = Zone 4	0 = no change in the ALS zone since the last read back of this register **(Default)** 1 = the ALS zone has changed. A read back of this	0 = INT Mode Disabled **(Default)** 1 = INT Mode Enabled

Table 26. Read-Back ADC Register (Address 0x37)

Bit 7 MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
Data	Data	Data	Data	Data	Data	Data	Data

This register contains the ADC data from the internal 8-bit ADC. This is a read-only register. When the ALS Interface is enabled this register is updated with the digitized ALS information every 140µs.

Table 27. Read-Average ADC Register (Address 0x38)

Bit 7 MSB	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 LSB
Data	Data	Data	Data	Data	Data	Data	Data

This register is updated after each average period.

Table 28. Brightness Registers (Addresses 0x40, 0x41, 0x42, 0x43, 0x44, 0x45)

Address	Function
0x40	Control Bank A Brightness Register (BREGA)
0x41	Control Bank B Brightness Register (BREGB)
0x42	Control Bank C High Brightness Register (BREGHC)
0x43	Control Bank D High Brightness Register (BREGHD)
0x44	Control Bank E High Brightness Register (BREGHE)
0x45	Control Bank F High Brightness Register (BREGHF)

Table 29. Brightness Registers Bit Description

Brightness Code Bits[7:0]
When the Mapping Mode is set for exponential mapping (Control Bank_Brightness Configuration Register Bit [2] = 0), the current approximates the equation: $I_{LED} = I_{LED\_FULLSCALE} \times 0.85^{\left[40-\left(\frac{Code+1}{6.4}\right)\right]}$ (9)
When the Mapping Mode is set for linear mapping (Control Bank_Brightness Configuration Register Bit [2] = 1), the current approximates the equation: $I_{LED} = I_{LED\_FULLSCALE} \times \frac{1}{255} \times Code$ (10)

Table 30. ALS Zone Boundary High And Low Registers (Addresses 0x50 - 0x57)

Address	Function
0x50	ALS Zone Boundary 0 High
0x51	ALS Zone Boundary 0 Low
0x52	ALS Zone Boundary 1 High
0x53	ALS Zone Boundary 1 Low
0x54	ALS Zone Boundary 2 High

Table 30. ALS Zone Boundary High And Low Registers (Addresses 0x50 - 0x57) (continued)

Address	Function
0x55	ALS Zone Boundary 2 Low
0x56	ALS Zone Boundary 3 High
0x57	ALS Zone Boundary 3 Low

Note: Each Zone Boundary register is 8 bits with a maximum voltage of 2 V. This gives a step size for each Zone Boundary Register bit of:

$$\text{ZoneBoundaryLSB} = \frac{2V}{255} = 7.8\ \text{mV} \tag{11}$$

Table 31. ALSM1 Zone Target Registers (Addresses 0x60 to 0x64)

Address	Function
0x60	ALSM1 Zone Target 0
0x61	ALSM1 Zone Target 1
0x62	ALSM1 Zone Target 2
0x63	ALSM1 Zone Target 3
0x64	ALSM1 Zone Target 4

Table 32. ALSM2 Zone Target Registers (Addresses 0x65 to 0x69)

Address	Function
0x65	ALSM2 Zone Target 0
0x66	ALSM2 Zone Target 1
0x67	ALSM2 Zone Target 2
0x68	ALSM2 Zone Target 3
0x69	ALSM2 Zone Target 4

Table 33. ALSM3 Zone Target Registers (Addresses 0x6A to 0x6E)

Address	Function
0x6A	ALSM3 Zone Target 0
0x6B	ALSM3 Zone Target 1
0x6C	ALSM3 Zone Target 2
0x6D	ALSM3 Zone Target 3
0x6E	ALSM3 Zone Target 4

When the Mapping Mode is set for exponential mapping (Control Bank_Brightness Configuration Register Bit [2] = 0), the current approximates Equation 12:

$$I_{LED} = I_{LED\_FULLSCALE} \times 0.85^{\left[40-\left(\frac{\text{Code}+1}{6.4}\right)\right]} \tag{12}$$

When the Mapping Mode is set for linear mapping (Control Bank_Brightness Configuration Register Bit [2] = 1), the current approximates Equation 13:

$$I_{LED} = I_{LED\_FULLSCALE} \times \frac{1}{255} \times \text{Code} \tag{13}$$

7.6.1.1 Pattern Generator Registers

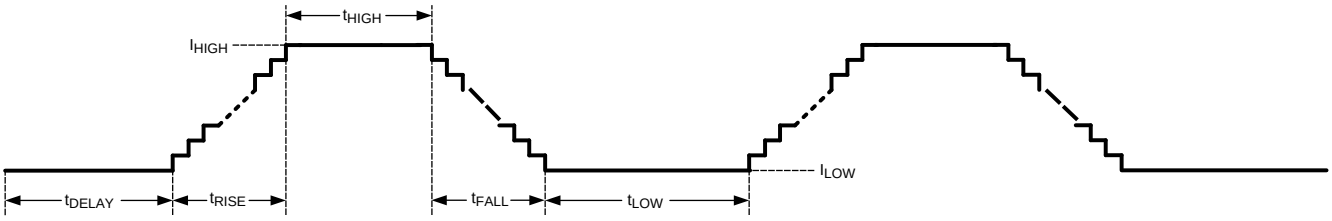


Figure 36. Pattern Generator Timing

Table 34. Pattern Generator Delay Registers (Addresses 0x70, 0x80, 0x90, 0xA0)

Address	Function
0x70	Pattern Generator 1 Delay Register
0x80	Pattern Generator 2 Delay Register
0x90	Pattern Generator 3 Delay Register
0xA0	Pattern Generator 4 Delay Register

Table 35. Pattern Generator Delay Register Bit Description

Bit 7 Not Used	Bit [6:0] t_{DELAY} times
	0x00 = 16.384ms (16.384ms/step) **(Default)**
	0x01 = 32.768ms
	:
	:
	0x3B = 983.05ms
	0x3C = 999.424ms
	0x3D = 1130.496ms (131.072ms/step)
	0x3E = 1261.568ms
	:
	:
	0x7F = 9781.248ms

Table 36. Pattern Generator Low-Time Registers (Addresses 0x71, 0x81, 0x91, 0xA1)

Address	Function
0x71	Pattern Generator 1 Low-Time Register
0x81	Pattern Generator 2 Low-Time Register
0x91	Pattern Generator 3 Low-Time Register
0xA1	Pattern Generator 4 Low-Time Register

Table 37. Pattern Generator Low-Time Register Bit Description

Bit [7:0]
t_{LOW} times
0x00 = 16.384ms (16.384ms/step) **(Default)**
0x01 = 32.768ms
:
:
0x3B = 983.05ms
0x3C = 999.424ms

Table 37. Pattern Generator Low-Time Register Bit Description (continued)

Bit [7:0]
0x3D = 1130.496ms (131.072ms/step)
0x3E = 1261.568ms
:
:
0x7F = 9781.248ms
0x80 = 10.305536s (524.288ms/step)
:
:
0xFF = 76.890112s

Table 38. Pattern Generator High-Time Registers (Addresses 0x72, 0x82, 0x92, 0xA2)

Address	Function
0x72	Pattern Generator 1 High-Time Register
0x82	Pattern Generator 2 High-Time Register
0x92	Pattern Generator 3 High-Time Register
0xA2	Pattern Generator 4 High-Time Register

Table 39. Pattern Generator High-Time Register Bit Description

Bit 7 Not Used	Bit [6:0] t_{HIGH} times
	0x00 = 16.384ms (16.384ms/step) **(Default)**
	0x01 = 32.768ms
	:
	:
	0x3B = 983.05ms
	0x3C = 999.424ms
	0x3D = 1130.496ms (131.072ms/step)
	0x3E = 1261.568ms
	:
	:
	0x7F = 9781.248ms

Table 40. Pattern Generator Low-Level Brightness Registers (Addresses 0x73, 0x83, 0x93, 0xA3)

Address	Function
0x73	Pattern Generator 1 Low-Level Brightness Register (BREGCL)
0x83	Pattern Generator 2 Low-Level Brightness Register (BREGDL)
0x93	Pattern Generator 3 Low-Level Brightness Register (BREGEL)
0xA3	Pattern Generator 4 Low-Level Brightness Register (BREGFL)

For Exponential Mapping Mode the low-level current becomes:

$$I_{LED\_LOW\_LEVEL} = I_{LED\_FULLSCALE} \times 0.85^{\left[40-\left(\frac{Code+1}{6.4}\right)\right]} \quad (14)$$

For Linear Mapping Mode the low-level current becomes:

$$I_{LED\_LOW\_LEVEL} = I_{LED\_FULLSCALE} \times \frac{1}{255} \times Code \quad (15)$$

Note: The Pattern Generator high level brightness setting is set through the Control Bank Brightness Registers (see Table 28).

Table 41. Pattern Generator Rise-Time Registers (Addresses 0x74, 0x84, 0x94, 0xA4)

Address	Function
0x74	Pattern Generator 1 Rise-Time Register
0x84	Pattern Generator 2 Rise-Time Register
0x94	Pattern Generator 3 Rise-Time Register
0xA4	Pattern Generator 4 Rise-TimeRegister

Table 42. Pattern Generator Rise-Time Register Bit Settings

Bits [7:3] Not Used	Bits [2:0] t_{RISE} (from I_{LOW} to I_{HIGH})
	000 = 2048µs **(Default)**
	001 = 262ms
	010 = 524ms
	011 = 1.049s
	100 = 2.097s
	101 = 4.194s
	110 = 8.389s
	111 = 16.78s

Table 43. Pattern Generator Fall-Time Registers (Addresses 0x75, 0x85, 0x95, 0xA5)

Address	Function
0x75	Pattern Generator 1 Fall-Time Register
0x85	Pattern Generator 2 Fall-Time Register
0x95	Pattern Generator 3 Fall-Time Register
0xA5	Pattern Generator 4 Fall-Time Register

Table 44. Pattern Generator Fall-Time Register Bit Settings

Bits [7:3] Not Used	Bits [2:0] t_{FALL} (from I_{HIGH} to I_{LOW})
	000 = 2048µs **(Default)**
	001 = 262ms
	010 = 524ms
	011 = 1.049s
	100 = 2.097s
	101 = 4.194s
	110 = 8.389s
	111 = 16.78s

Table 45. Led String Open Fault Readback Register (Address 0xB0)

Bit 7 (Not Used)	Bit 6 (LVLED5 Open)	Bit 5 (LVLED4 Open)	Bit 4 (LVLED3 Open)	Bit 3 (LVLED2 Open)	Bit 2 (LVLED1 Open)	Bit 1 (HVLED2 Open)	Bit 0 (HVLED1 Open)
	0 = Normal Operation 1 = Open	0 = Normal Operation 1 = Open	0 = Normal Operation 1 = Open	0 = Normal Operation 1 = Open	0 = Normal Operation 1 = Open	0 = Normal Operation 1 = Open	0 = Normal Operation 1 = Open

Table 46. LED String Short Fault Readback Register (Address 0xB1)

Bit 7 (Not Used)	Bit 6 (LVLED5 Short)	Bit 5 (LVLED4 Short)	Bit 4 (LVLED3 Short)	Bit 3 (LVLED2 Short)	Bit 2 (LVLED1 Short)	Bit 1 (HVLED2 Short)	Bit 0 (HVLED1 Short)
	0 = Normal Operation 1 = Short	0 = Normal Operation 1 = Short	0 = Normal Operation 1 = Short	0 = Normal Operation 1 = Short	0 = Normal Operation 1 = Short	0 = Normal Operation 1 = Short	0 = Normal Operation 1 = Short

Table 47. LED Fault Enable (Address 0xB2)

Bits [7:2] Not Used	Bits [1] LED Short Fault Enable	Bit 0 LED Open Fault Enable
N/A	0 = Short Faults Disabled **(Default)** 1 = Short Faults Enabled	0 = Open Faults Disabled **(Default)** 1 = Open Faults Enabled

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM3533 is a dual-string (up to 40 V at up to 30 mA) backlight driver with five integrated low voltage indicator current sinks. The current through any LED can be controlled by the I^2C bus, the PWM input, or via an external ambient light sensor. Any low voltage current sink can be made to blink via a programmable pattern. The programmable pattern can have variable high pulse time, low pulse time, delay from start, high time current, low time current, and ramp rates. The device operates from a typical V_{IN} from 2.7 V to 5.5 V, and an ambient temperature range of -40°C to +85°C.

8.2 Typical Application

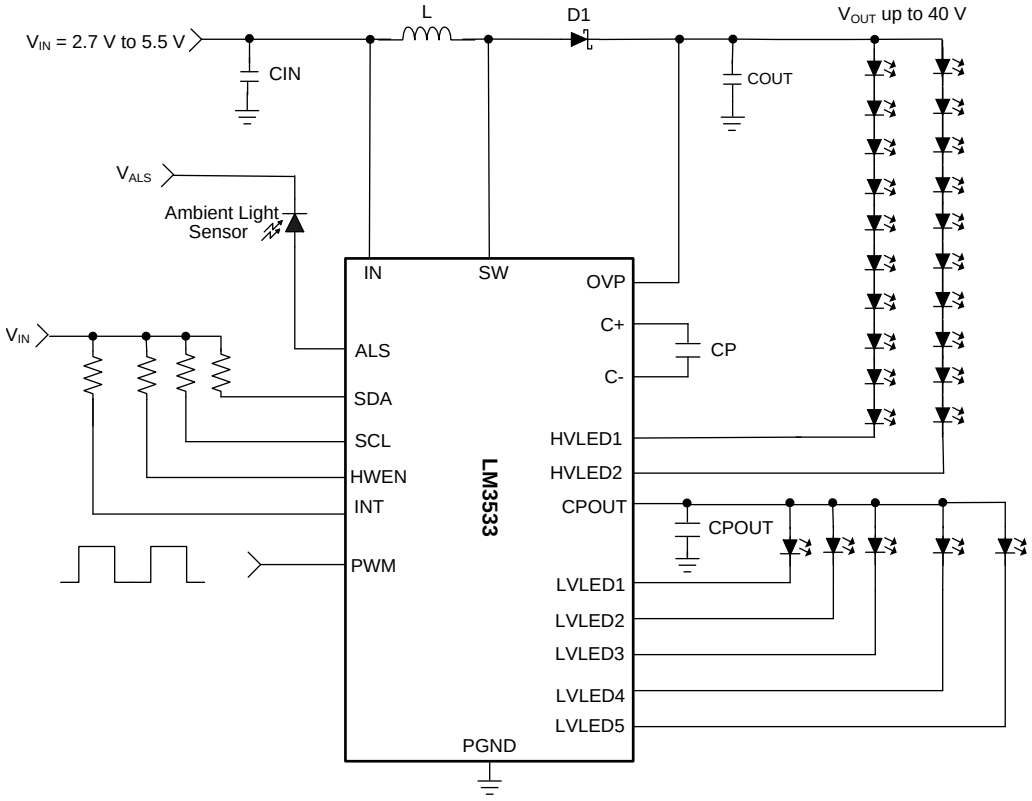


Figure 37. LM3533 Typical Application

Typical Application (continued)

8.2.1 Design Requirements

For typical lighting power-source applications, use the parameters listed in Table 48.

Table 48. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Minimum input voltage	2.7 V
Minimum output voltage	0.6 V
Output current	0 to 750 mA
Switching frequency	2.4 MHz (typical)

8.2.2 Detailed Design Procedure

Table 49. Application Circuit Component List

COMPONENT	MANUFACTURER	VALUE	PART NUMBER	SIZE (mm)	CURRENT/VOLTAGE RATING (RESISTANCE)
L	TDK	10 µH	VLF302512MT-100M	2.5 x 3 x 1.2	620 mA/0.25 Ω
COUT	TDK	1 µF	C2012X5R1H105	0805	50 V
CIN	TDK	2.2 µF	C1005X5R1A225	0402	10 V
CPOUT/CP	TDK	1 µF	C1005X5R1A105	0402	10 V
Diode	On-Semi	Schottky	NSR0240V2T1G	SOD-523	40 V, 250 mA

8.2.2.1 Boost Converter Maximum Output Power (Boost)

The LM3533 maximum output power is governed by two factors: the peak current limit (I_{CL} = 880 mA minimum), and the maximum output voltage (V_{OVP}). When the application causes either of these limits to be reached, it is possible that the proper current regulation and matching between LED current strings may not be met.

8.2.2.2 Peak Current Limited

In the case of a peak current limited situation, when the peak of the inductor current hits the LM3533 current limit, the NFET switch turns off for the remainder of the switching period. If this happens each switching cycle the LM3533 regulates the peak of the inductor current instead of the headroom across the current sinks. This can result in the dropout of the boost output connected current sinks, and the LED current dropping below its programmed level.

The peak current in a boost converter is dependent on the value of the inductor, total LED current in the boost (I_{OUT}), the boost output voltage (V_{OUT}) (which is the highest voltage LED string + 0.4 V regulated headroom voltage), the input voltage (V_{IN}), the switching frequency, and the efficiency (Output Power/Input Power). Additionally, the peak current is different depending on whether the inductor current is continuous during the entire switching period (CCM), or discontinuous (DCM) where it goes to 0 before the switching period ends. For Continuous Conduction Mode the peak inductor current is given by:

$$IPEAK = \frac{IOUT \times VOUT}{VIN \times efficiency} + \left[\frac{VIN}{2 \times f_{SW} \times L} \times \left(1 - \frac{VIN \times efficiency}{VOUT}\right)\right] \quad (16)$$

For DCM the peak inductor current is given by:

$$I_{PEAK} = \sqrt{\frac{2 \times I_{OUT}}{f_{SW} \times L \times efficiency} \times \left(V_{OUT} - V_{IN} \times efficiency\right)} \quad (17)$$

To determine which mode the circuit is operating in (CCM or DCM) it is necessary to perform a calculation to test whether the inductor current ripple is less than the anticipated input current (I_{IN}). If ΔI_L is less than I_{IN} then the device is operating in CCM. If ΔI_L is greater than I_{IN} then the device is operating in DCM.

$$\frac{I_{OUT} \times V_{OUT}}{V_{IN} \times efficiency} > \frac{V_{IN}}{f_{SW} \times L} \times \left(1 - \frac{V_{IN} \times efficiency}{V_{OUT}}\right) \quad (18)$$

Typically at currents high enough to reach the LM3533 device's peak current limit, the device is operating in CCM. When choosing the switching frequency and the inductor value, Equation 16 and Equation 17 must be used to ensure that I_{PEAK} stays below I_{CL_MIN} (see *Electrical Characteristics*).

8.2.2.3 Output Voltage Limited

In the case of a output voltage limited situation, when the boost output voltage hits the LM3533 OVP threshold, the NFET turns off and stays off until the output voltage falls below the hysteresis level (typically 1 V below the OVP threshold). This results in the boost converter regulating the output voltage to the programmed OVP threshold (16 V, 24 V, 32 V, or 40 V), causing the current sinks to go into dropout. The default OVP threshold is set at 16 V. For LED strings higher than typically 4 series LEDs, the OVP has to be programmed higher after power-up or after a HWEN reset.

8.2.2.4 Maximum Output Power (Charge Pump)

The maximum output power available from the LM3533 charge pump is determined by the maximum output voltage available from the charge pump. In 1× gain the charge pump operates in Pass Mode so that the voltage at CPOUT tracks V_{IN} (less the drop across the charge pumps pass switch). In this case the maximum output power is given as:

$$P_{OUT\_MAX} = I_{LVLED\_TOTAL} \times (V_{IN} - I_{LVLED\_TOTAL} \times R_{CP}) \quad (19)$$

where

- R_{CP} is the resistance from IN to CPOUT
- I_{LVLED_TOTAL} is the maximum programmed current in the LVLED strings.

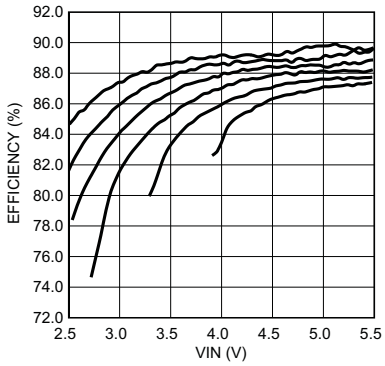
In 2× gain the voltage at CPOUT (V_{CPOUT_2X}) is regulated to typically 4.4 V. In this case the maximum output power is given by:

$$P_{OUT\_MAX} = I_{LVLED\_TOTAL} \times V_{CPOUT\_2X} \quad (20)$$

Equation 19 and Equation 20 both assume there is sufficient headroom at the top side of the low-voltage current sinks to ensure the LED current remains in regulation (V_{HR_LV}) in the *Electrical Characteristics*.

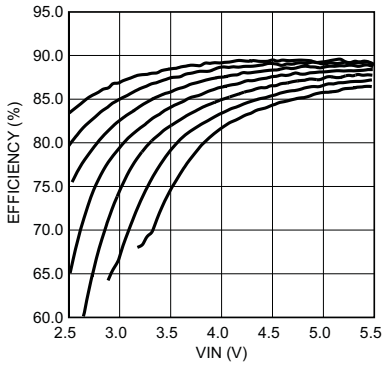
8.2.3 Application Curves

V_{IN} = 3.6 V, LEDs are WLEDs part number SML-312WBCW(A), typical application circuit with L = TDK (VLF302512, 4.7 µH, 10 µH, 22 µH where specified), Schottky = On-Semi (NSR0240V2T1G), T_A = 25°C, unless otherwise specified. Efficiency is given as $V_{OUT} \times (I_{HVLED1} + I_{HVLED2})/(V_{IN} \times I_{IN})$; matching curves are given as $(\Delta I_{LED\_MAX}/I_{LED\_AVE})$.



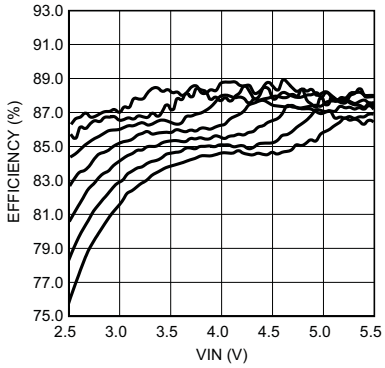
L = 22 µH 20 mA/String f_{SW} = 500 kHz
Top To Bottom: 2×4, 2×5, 2×6, 2×7, 2×8, 2×9 (LEDs)

Figure 38. Efficiency vs V_{IN}, Dual String



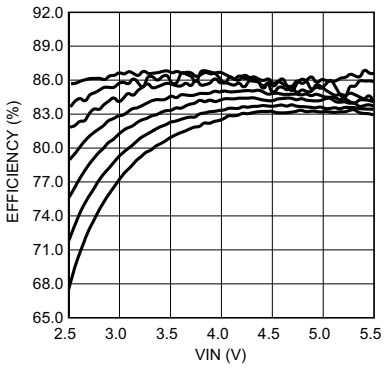
L = 22 µH 20 mA/String f_{SW} = 1 MHz
Top To Bottom: 2×4, 2×5, 2×6, 2×7, 2×8, 2×9, 2×10 (LEDs)

Figure 39. Efficiency vs V_{IN}, Dual String



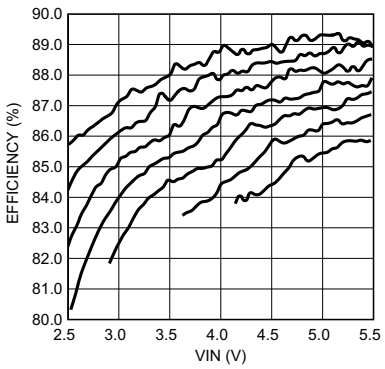
L = 22 µH 20 mA/String f_{SW} = 500 kHz
Top To Bottom: 1×4, 1×5, 1×6, 1×7, 1×8, 1×9, 1×10 (LEDs)

Figure 40. Efficiency vs V_{IN}, Single String



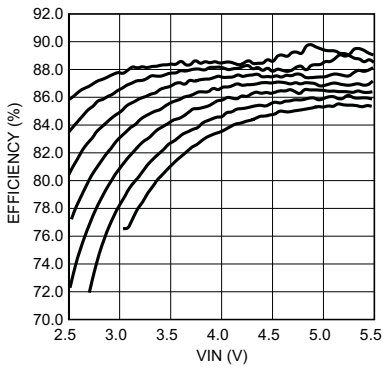
L = 22 µH 20 mA/String f_{SW} = 1 MHz
Top To Bottom: 1×4, 1×5, 1×6, 1×7, 1×8, 1×9, 1×10 (LEDs)

Figure 41. Efficiency vs V_{IN}, Single String



L = 10 µH 20 mA/String f_{SW} = 500 kHz
Top To Bottom: 2×4, 2×5, 2×6, 2×7, 2×8, 2×9 (LEDs)

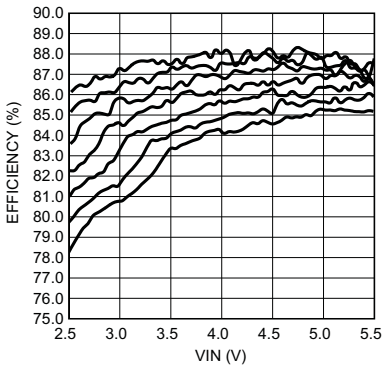
Figure 42. Efficiency vs V_{IN}, Dual String



L = 10 µH 20 mA/String f_{SW} = 1 MHz
Top To Bottom: 2×4, 2×5, 2×6, 2×7, 2×8, 2×9, 2×10 (LEDs)

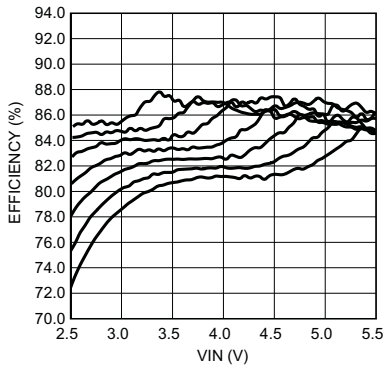
Figure 43. Efficiency vs V_{IN}, Dual String

V_{IN} = 3.6 V, LEDs are WLEDs part number SML-312WBCW(A), typical application circuit with L = TDK (VLF302512, 4.7 µH, 10 µH, 22 µH where specified), Schottky = On-Semi (NSR0240V2T1G), T_A = 25°C, unless otherwise specified. Efficiency is given as $V_{OUT} \times (I_{HVLED1} + I_{HVLED2})/(V_{IN} \times I_{IN})$; matching curves are given as $(\Delta I_{LED\_MAX}/I_{LED\_AVE})$.



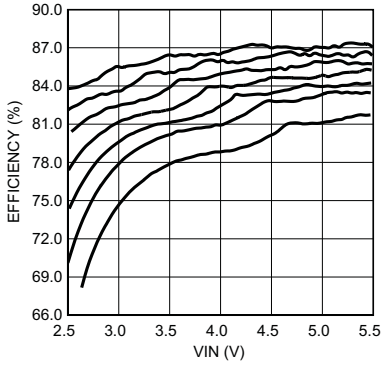
L = 10 µH 20 mA/String f_{SW} = 500 kHz
Top To Bottom: 1×4, 1×5, 1×6, 1×7, 1×8, 1×9, 1×10 (LEDs)

Figure 44. Efficiency vs V_{IN}, Single String



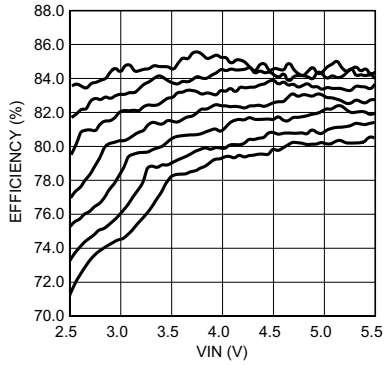
L = 10 µH 20 mA/String f_{SW} = 1 MHz
Top To Bottom: 1×4, 1×5, 1×6, 1×7, 1×8, 1×9, 1×10 (LEDs)

Figure 45. Efficiency vs V_{IN}, Single String



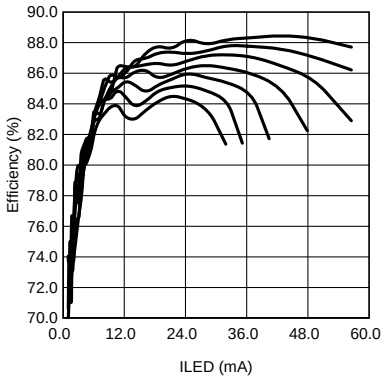
L = 4.7 µH 20 mA/String f_{SW} = 1 MHz
Top To Bottom: 2×4, 2×5, 2×6, 2×7, 2×8, 2×9 (LEDs)

Figure 46. Efficiency vs V_{IN}, Dual String



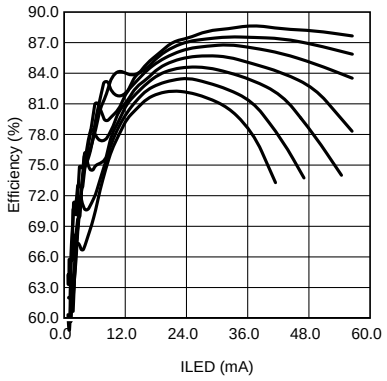
L = 4.7 µH 20 mA/String
Top To Bottom: 1×4, 1×5, 1×6, 1×7, 1×8, 1×9, 1×10 (LEDs)

Figure 47. Efficiency vs V_{IN}, Single String



L = 22 µH V_{IN} = 3.6 V f_{SW} = 500 kHz
Top To Bottom: 1×4, 1×5, 1×6, 1×7, 1×8, 1×9, 1×10 (LEDs)

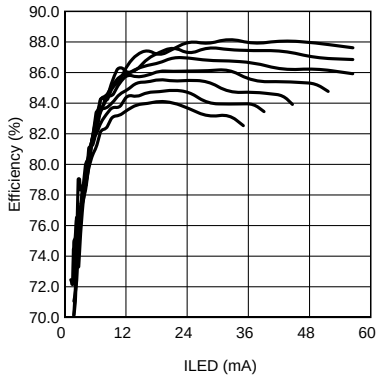
Figure 48. Efficiency vs I_{LED}



L = 22 µH V_{IN} = 3.6 V f_{SW} = 1 MHz
Top To Bottom: 2×4, 2×5, 2×6, 2×7, 2×8, 2×9, 2×10 (LEDs)

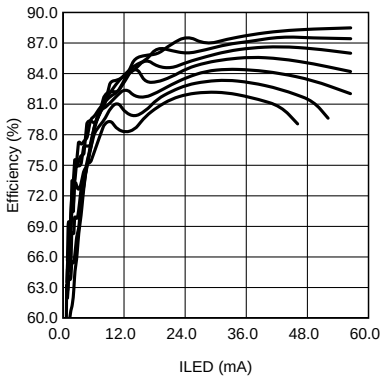
Figure 49. Efficiency vs I_{LED}

V_{IN} = 3.6 V, LEDs are WLEDs part number SML-312WBCW(A), typical application circuit with L = TDK (VLF302512, 4.7 µH, 10 µH, 22 µH where specified), Schottky = On-Semi (NSR0240V2T1G), T_A = 25°C, unless otherwise specified. Efficiency is given as $V_{OUT} \times (I_{HVLED1} + I_{HVLED2})/(V_{IN} \times I_{IN})$; matching curves are given as $(\Delta I_{LED\_MAX}/I_{LED\_AVE})$.



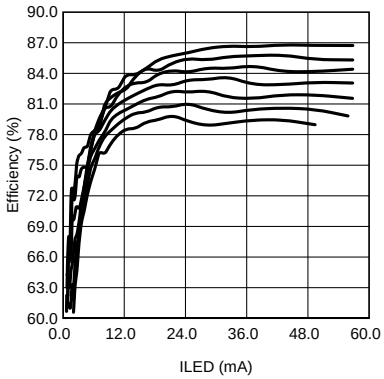
L = 10 µH V_{IN} = 3.6 V f_{SW} = 500 kHz
Top To Bottom: 2×4, 2×5, 2×6, 2×7, 2×8, 2×9, 2×10 (LEDs)

Figure 50. Efficiency vs I_{LED}



L = 10 µH V_{IN} = 3.6 V f_{SW} = 1 MHz
Top To Bottom: 2×4, 2×5, 2×6, 2×7, 2×8, 2×9, 2×10 (LEDs)

Figure 51. Efficiency vs I_{LED}



L = 4.7 µH V_{IN} = 3.6 V f_{SW} = 1 MHz
Top To Bottom: 2×4, 2×5, 2×6, 2×7, 2×8, 2×9, 2×10 (LEDs)

Figure 52. Efficiency vs I_{LED}

9 Power Supply Recommendations

The LM3532 is designed to operate from an input supply range of 2.7 V to 5.5 V. This input supply must be well-regulated and provide the peak current required by the LED configuration and inductor selected.

10 Layout

10.1 Layout Guidelines

10.1.1 Boost

The LM3533 inductive boost converter sees a high switched voltage (up to 40 V) at the SW pin, and a step current (up to 1 A) through the Schottky diode and output capacitor each switching cycle. The high switching voltage can create interference into nearby nodes due to electric field coupling (I = CdV/dt). The large step current through the diode and the output capacitor can cause a large voltage spike at the SW pin and the OVP pin due to parasitic inductance in the step current conducting path (V = Ldi/dt). Board layout guidelines are geared towards minimizing this electric field coupling and conducted noise. Figure 53 highlights these two noise-generating components.

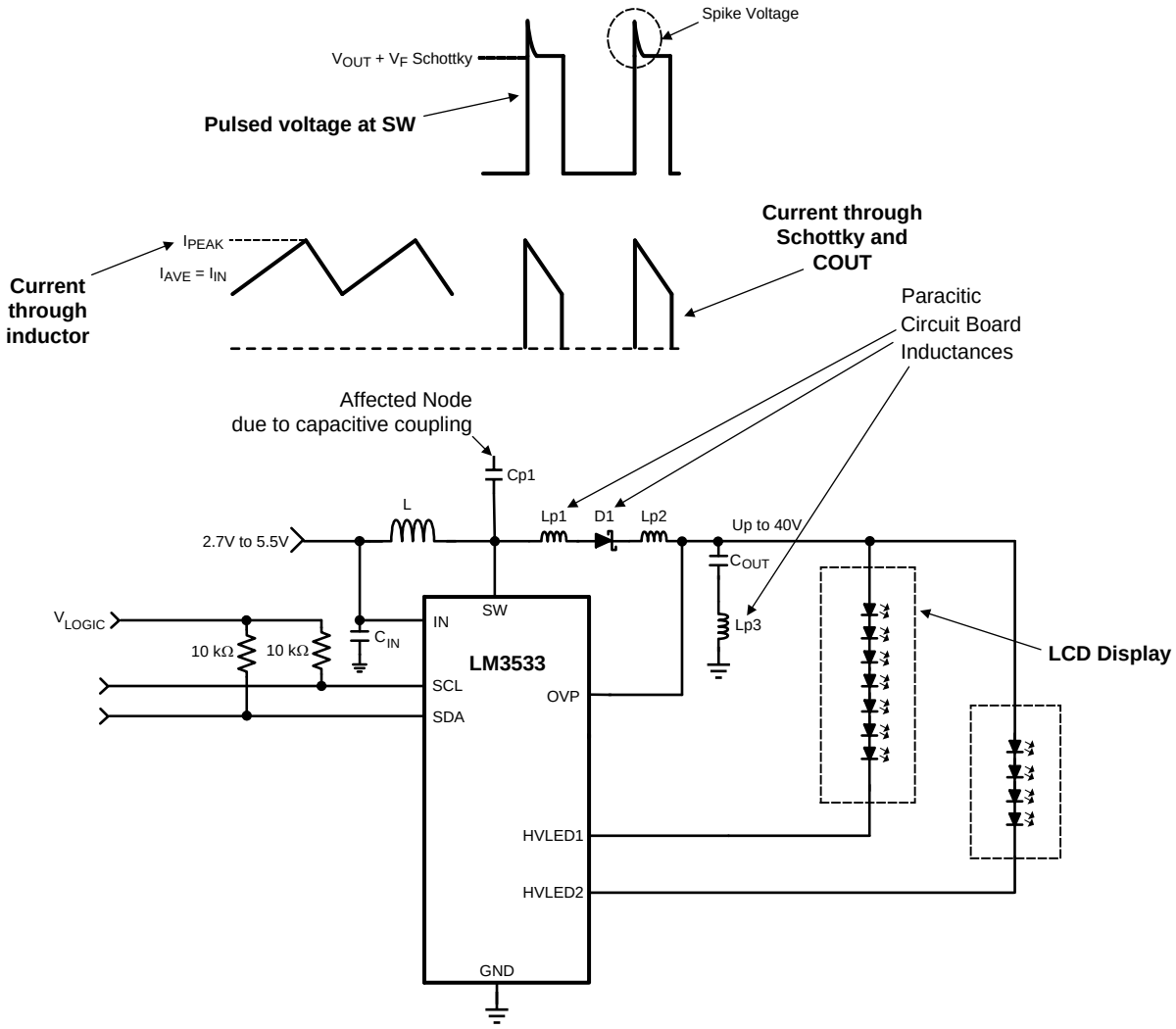


Figure 53. LM3533 Inductive Boost Converter Showing Pulsed Voltage at SW (High Dv/Dt) and Current Through Schottky and C_{OUT}(High Di/Dt)

The following list details the main (layout sensitive) areas of the LM3533 inductive boost converter in order of decreasing importance:

1. Output Capacitor:
   - Schottky Cathode to COUT+
   - COUT− to GND

Layout Guidelines (continued)

2. Schottky Diode:
   – SW Pin to Schottky Anode
   – Schottky Cathode to COUT+
3. Inductor:
   – SW Node PCB capacitance to other traces
4. Input Capacitor:
   – CIN+ to IN pin

10.1.1.1 Boost Output Capacitor Selection and Placement

The LM3533 inductive boost converter requires a 1-µF output capacitor. The voltage rating of the capacitor depends on the selected OVP setting. For the 16-V setting a 16-V capacitor must be used. For the 24-V setting a 25-V capacitor must be used. For the 32-V setting, a 35-V capacitor must be used. For the 40-V setting a 50-V capacitor must be used. Pay careful attention to the capacitor's tolerance and DC bias response. For proper operation the degradation in capacitance due to tolerance, DC bias, and temperature, must stay above 0.4 µF. This might require placing two devices in parallel in order to maintain the required output capacitance over the device operating range, and series LED configuration.

Because the output capacitor is in the path of the inductor current discharge path, a high-current step from 0 to I_{PEAK} is seen each time the switch turns off and the Schottky diode turns on. Any inductance along this series path from the cathode of the diode through C_{OUT} and back into the LM3533 GND pin contributes to voltage spikes (V_{SPIKE} = LP_ × dI/dt) at SW and OUT. These spikes can potentially over-voltage the SW pin, or feed through to GND. To avoid this, COUT+ must be connected as closely as possible to the cathode of the Schottky diode, and COUT− must be connected as closely as possible to the LM3533 device's GND pin. The best placement for COUT is on the same layer as the LM3533 to avoid any vias that can add excessive series inductance.

10.1.1.2 Schottky Diode Placement

The Schottky diode must have a reverse breakdown voltage greater than the LM3533 maximum output voltage (see *Overvoltage Protection (Inductive Boost)*). Additionally, the diode must have an average current rating high enough to handle the LM3533's maximum output current, and at the same time the diode's peak current rating must be high enough to handle the peak inductor current. Schottky diodes are required due to their lower forward voltage drop (0.3 V to 0.5 V) and their fast recovery time.

In the LM3533 boost circuit the Schottky diode is in the path of the inductor current discharge; thus, the Schottky diode sees a high-current step from 0 to I_{PEAK} each time the switch turns off and the diode turns on. Any inductance in series with the diode causes a voltage spike (V_{SPIKE} = LP_ × dI/dt) at SW and OUT. This can potentially over-voltage the SW pin, or feed through to V_{OUT} and through the output capacitor and into GND. Connecting the anode of the diode as closely as possible to the SW pin and the cathode of the diode as closely as possible to COUT+ reduces the inductance (LP_) and minimize these voltage spikes.

10.1.1.3 Inductor Placement

The node where the inductor connects to the LM3533's SW pin has 2 issues. First, a large switched voltage (0 to V_{OUT} + $V_{F\_SCHOTTKY}$) appears on this node every switching cycle. This switched voltage can be capacitively coupled into nearby nodes. Second, there is a relatively large current (input current) on the traces connecting the input supply to the inductor and connecting the inductor to the SW pin. Any resistance in this path can cause voltage drops that can negatively affect efficiency and reduce the input operating voltage range.

To reduce the capacitive coupling of the signal on SW into nearby traces, the SW pin-to-inductor connection must be minimized in area. This limits the PCB capacitance from SW to other traces. Additionally, high-impedance nodes that are more susceptible to electric field coupling need to be routed away from SW and not directly adjacent or beneath. This is especially true for traces such as SCL, SDA, HWEN, PWM, and possibly ALS. A GND plane placed directly below SW dramatically reduces the capacitance from SW into nearby traces.

Lastly, limit the trace resistance of the VBATT-to-inductor connection and from the inductor-to-SW connection, by use of short, wide traces.

Layout Guidelines (continued)

10.1.1.4 Boost Input Capacitor Selection and Placement

The input capacitor on the LM3533 filters the voltage ripple due to the switching action of the inductive boost and the capacitive charge pump doubler. A ceramic capacitor of at least 2.2 µF must be used.

For the LM3533 boost converter, the input capacitor filters the inductor current ripple and the internal MOSFET driver currents during turn on of the internal power switch. The driver current requirement can range from 50 mA at 2.7 V to over 200 mA at 5.5 V with fast durations of approximately 10 ns to 20 ns. This appears as high di/dt current pulses coming from the input capacitor each time the switch turns on. Close placement of the input capacitor to the IN pin and to the GND pin is critical because any series inductance between IN and CIN+ or CIN− and GND can create voltage spikes that could appear on the V_{IN} supply line and in the GND plane.

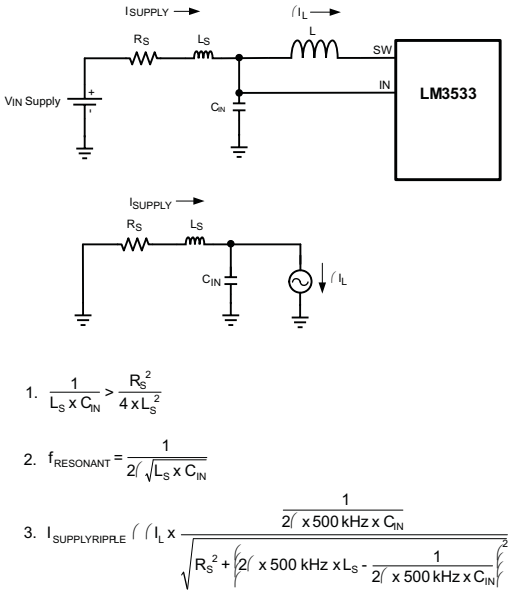
Close placement of the input bypass capacitor at the input side of the inductor is also critical. The source impedance (inductance and resistance) from the input supply, along with the input capacitor of the LM3533, form a series RLC circuit. If the output resistance from the source (R_S) is low enough the circuit is underdamped and has a resonant frequency (typically the case). Depending on the size of L_S the resonant frequency could occur below, close to, or above the LM3533 switching frequency. This can cause the supply current ripple to be:

1. Approximately equal to the inductor current ripple when the resonant frequency occurs well above the LM3533 switching frequency;
2. Greater than the inductor current ripple when the resonant frequency occurs near the switching frequency; or
3. Less than the inductor current ripple when the resonant frequency occurs well below the switching frequency. Figure 54 shows the series RLC circuit formed from the output impedance of the supply and the input capacitor.

The circuit is redrawn for the AC case where the V_{IN} supply is replaced with a short to GND, and the LM3533 plus inductor is replaced with a current source (ΔI_L). Equation 1 is the criteria for an underdamped response. Equation 2 is the resonant frequency. Equation 3 is the approximated supply current ripple as a function of LS, RS, and CIN.

As an example, consider a 3.6-V supply with 0.1 Ω of series resistance connected to C_{IN} through 50 nH of connecting traces. This results in an under-damped input-filter circuit with a resonant frequency of 712 kHz. Because both the 1-MHz and 500-kHz switching frequency options lie close to the resonant frequency of the input filter, the supply current ripple is probably larger than the inductor current ripple. In this case, using equation 3, the supply current ripple can be approximated as 1.68 times the inductor current ripple (using a 500-kHz switching frequency) and 0.86 times the inductor current ripple using a 1-MHz switching frequency. Increasing the series inductance (L_S) to 500 nH causes the resonant frequency to move to around 225 kHz, and the supply current ripple to be approximately 0.25 times the inductor current ripple (500-kHz switching frequency) and 0.053 times for a 1-MHz switching frequency.

Layout Guidelines (continued)



1. $\frac{1}{L_S \times C_{IN}} > \frac{R_S^2}{4 \times L_S^2}$
2. $f_{RESONANT} = \frac{1}{2\sqrt{L_S \times C_{IN}}}$
3. $I_{SUPPLYRIPPLE} \approx I_L \times \frac{\frac{1}{2\pi \times 500\,kHz \times C_{IN}}}{\sqrt{R_S^2 + \left(2\pi \times 500\,kHz \times L_S - \frac{1}{2\pi \times 500\,kHz \times C_{IN}}\right)^2}}$

Figure 54. Input RLC Network

10.1.2 Charge Pump

The charge pump basically has three areas of concern regarding component placement:

1. The flying capacitor (CP)
2. The output capacitor (CPOUT)
3. The input capacitor

10.1.2.1 Flying Capacitor (CP)

The charge pump flying capacitor must quickly charge up to the input voltage and then supply the current to the output every switching cycle. Because the charge pump switching frequency is 1 MHz, the capacitor must be a low-inductance and low-resistive ceramic. Additionally, there must be a low-inductive connection from CP to the LM3533 flying capacitor terminals C+ and C−. This is accomplished by placing CP as close as possible to the LM3533 and on the same layer to avoid vias.

10.1.2.2 Output Capacitor (CPOUT)

The charge pump output capacitor sees the switched charge from the flying capacitor every switching cycle (1 MHz). This fast switching action requires that a low inductive and low resistive capacitor (ceramic) be used and that CPOUT be connected to the LM3533 CPOUT pin with a low inductive connection. This is done by placing CPOUT as close as possible to the CPOUT and GND pins of the LM3533 and on the same layer as the LM3533 to avoid vias.

10.1.2.3 Charge Pump Input Capacitor Placement

The input capacitor for the LM3533 charge pump is the same one used for the LM3533 inductive boost converter (see *Boost Input Capacitor Selection and Placement*).

10.2 Layout Example

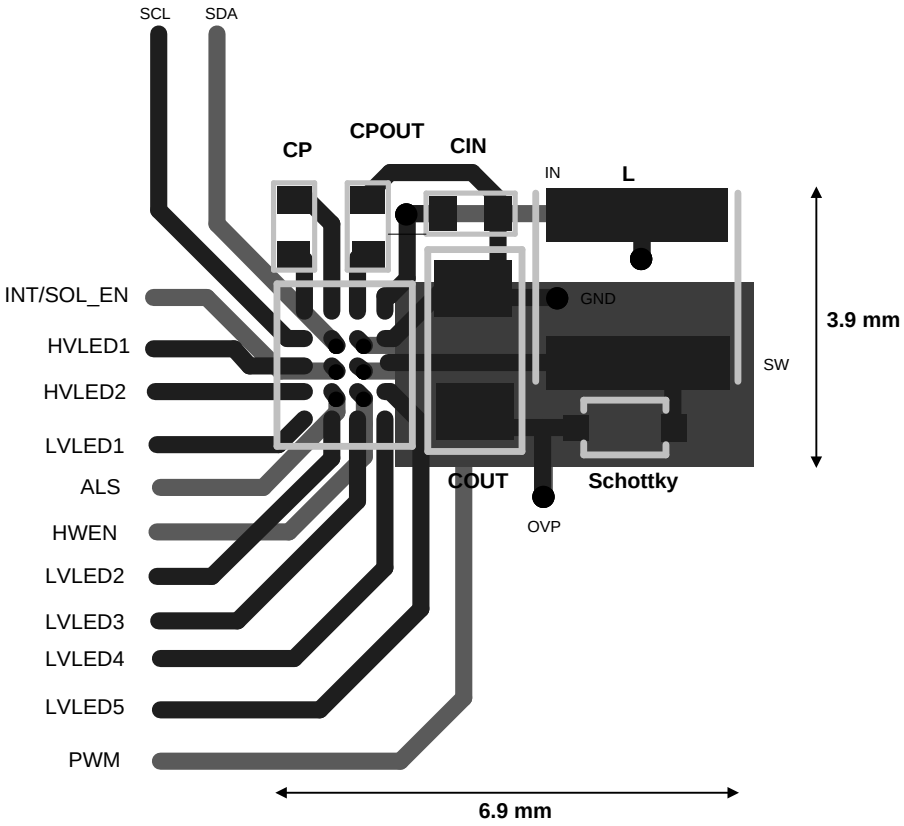


Figure 55. LM3533 Example Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.2 Related Documentation

For additional information, see the following:

TI Application Note AN-1112 *DSBGA Wafer Level Chip Scale Package* (SNVA009).

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3533TME-40/NOPB	ACTIVE	DSBGA	YFQ	20	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	D72B	Samples
LM3533TME-40A/NOPB	ACTIVE	DSBGA	YFQ	20	250	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	D74B	Samples
LM3533TMX-40/NOPB	ACTIVE	DSBGA	YFQ	20	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	D72B	Samples
LM3533TMX-40A/NOPB	ACTIVE	DSBGA	YFQ	20	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	D74B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

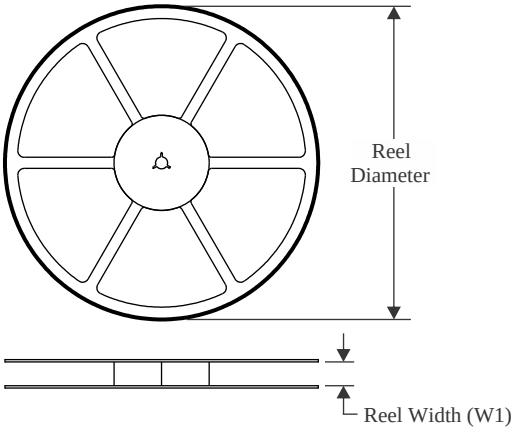
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

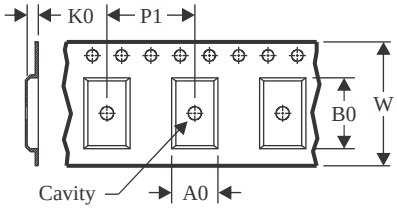
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

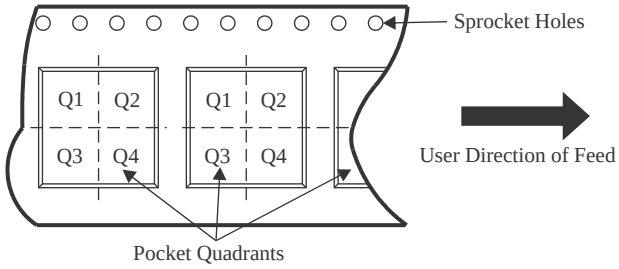


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

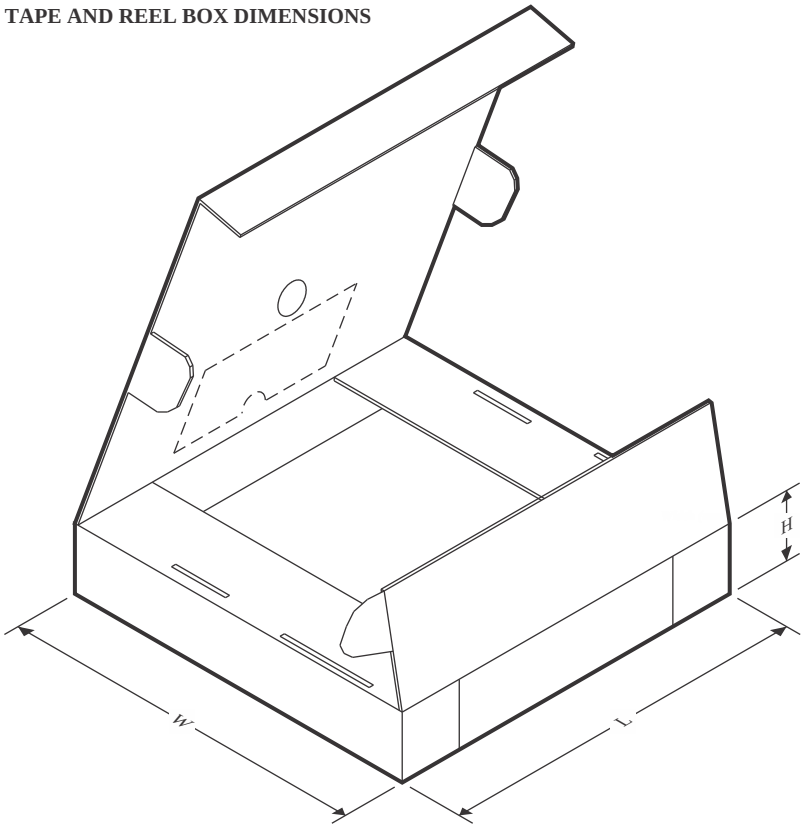
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3533TME-40/NOPB	DSBGA	YFQ	20	250	178.0	8.4	1.89	2.2	0.76	4.0	8.0	Q1
LM3533TME-40A/NOPB	DSBGA	YFQ	20	250	178.0	8.4	1.89	2.2	0.76	4.0	8.0	Q1
LM3533TMX-40/NOPB	DSBGA	YFQ	20	3000	178.0	8.4	1.89	2.2	0.76	4.0	8.0	Q1
LM3533TMX-40A/NOPB	DSBGA	YFQ	20	3000	178.0	8.4	1.89	2.2	0.76	4.0	8.0	Q1

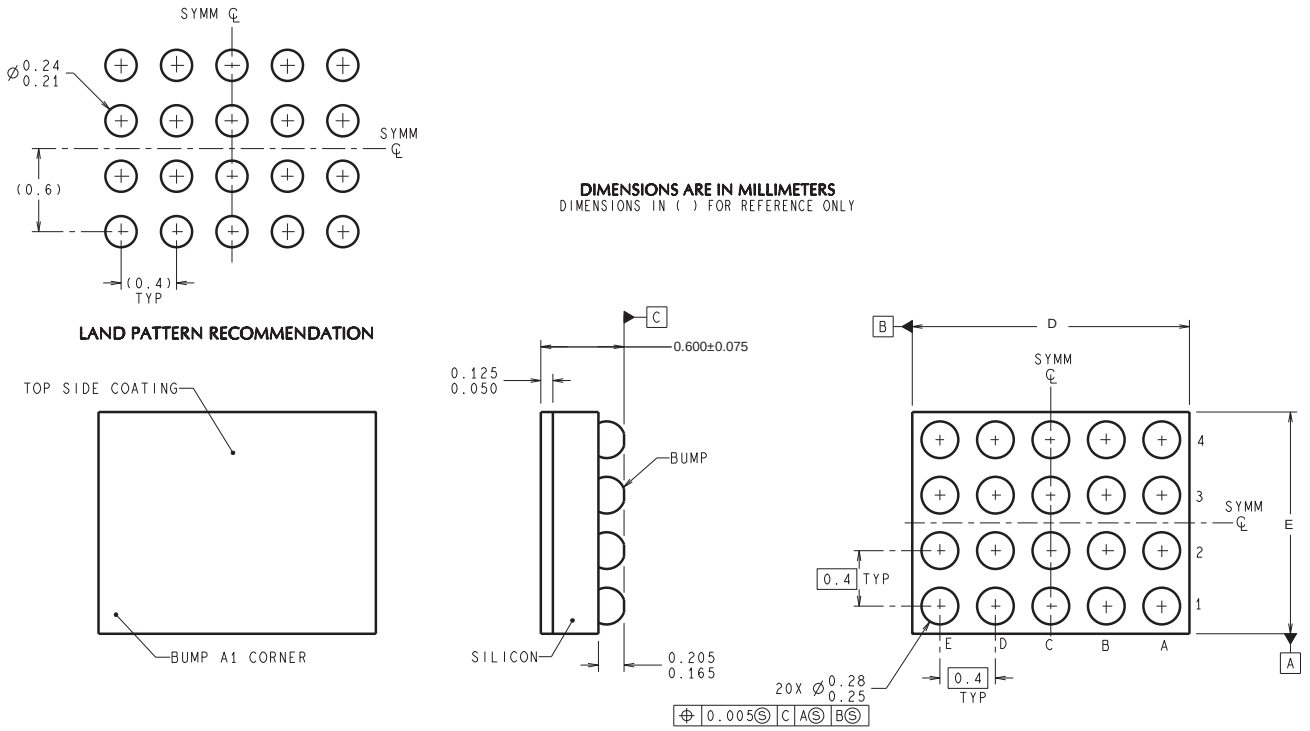
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3533TME-40/NOPB	DSBGA	YFQ	20	250	208.0	191.0	35.0
LM3533TME-40A/NOPB	DSBGA	YFQ	20	250	208.0	191.0	35.0
LM3533TMX-40/NOPB	DSBGA	YFQ	20	3000	208.0	191.0	35.0
LM3533TMX-40A/NOPB	DSBGA	YFQ	20	3000	208.0	191.0	35.0

YFQ0020



D: Max = 2.04 mm, Min = 1.98 mm

E: Max = 1.78 mm, Min = 1.72 mm

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NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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